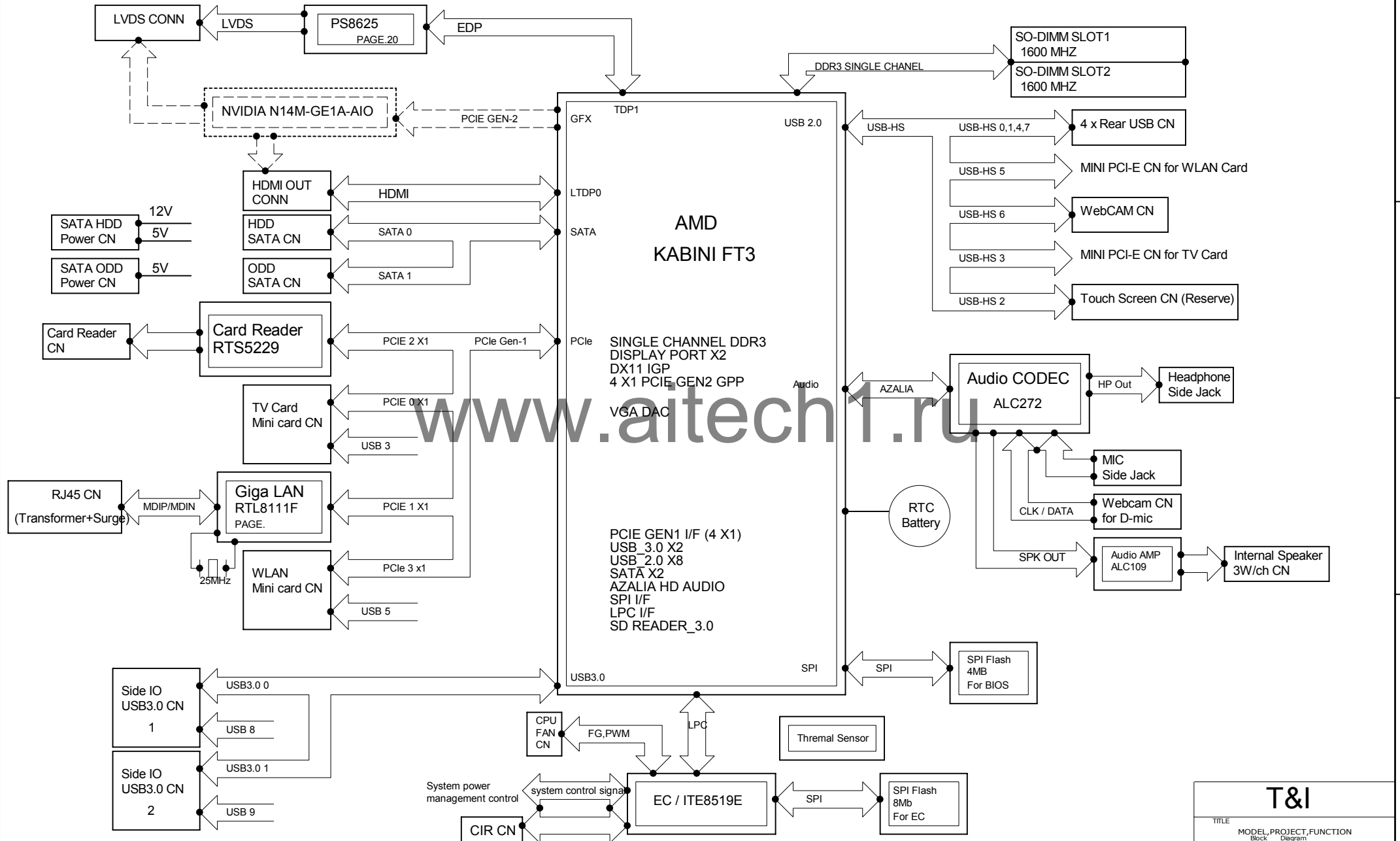




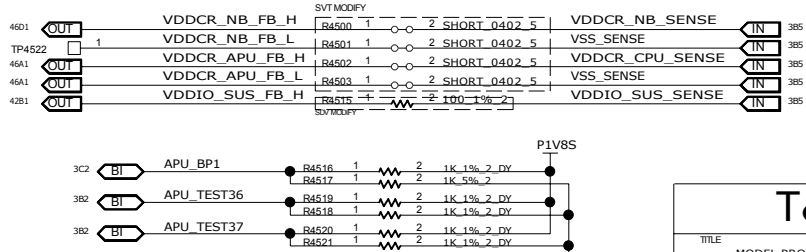
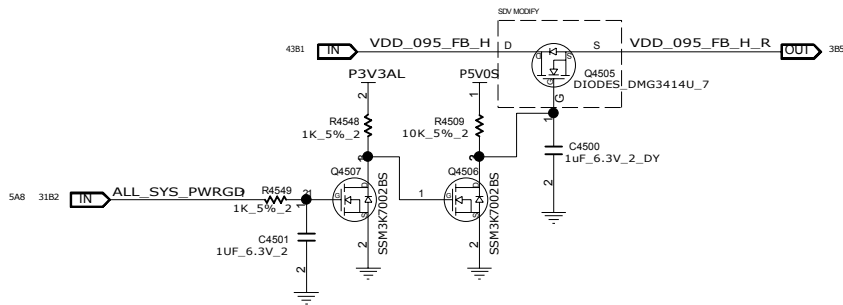
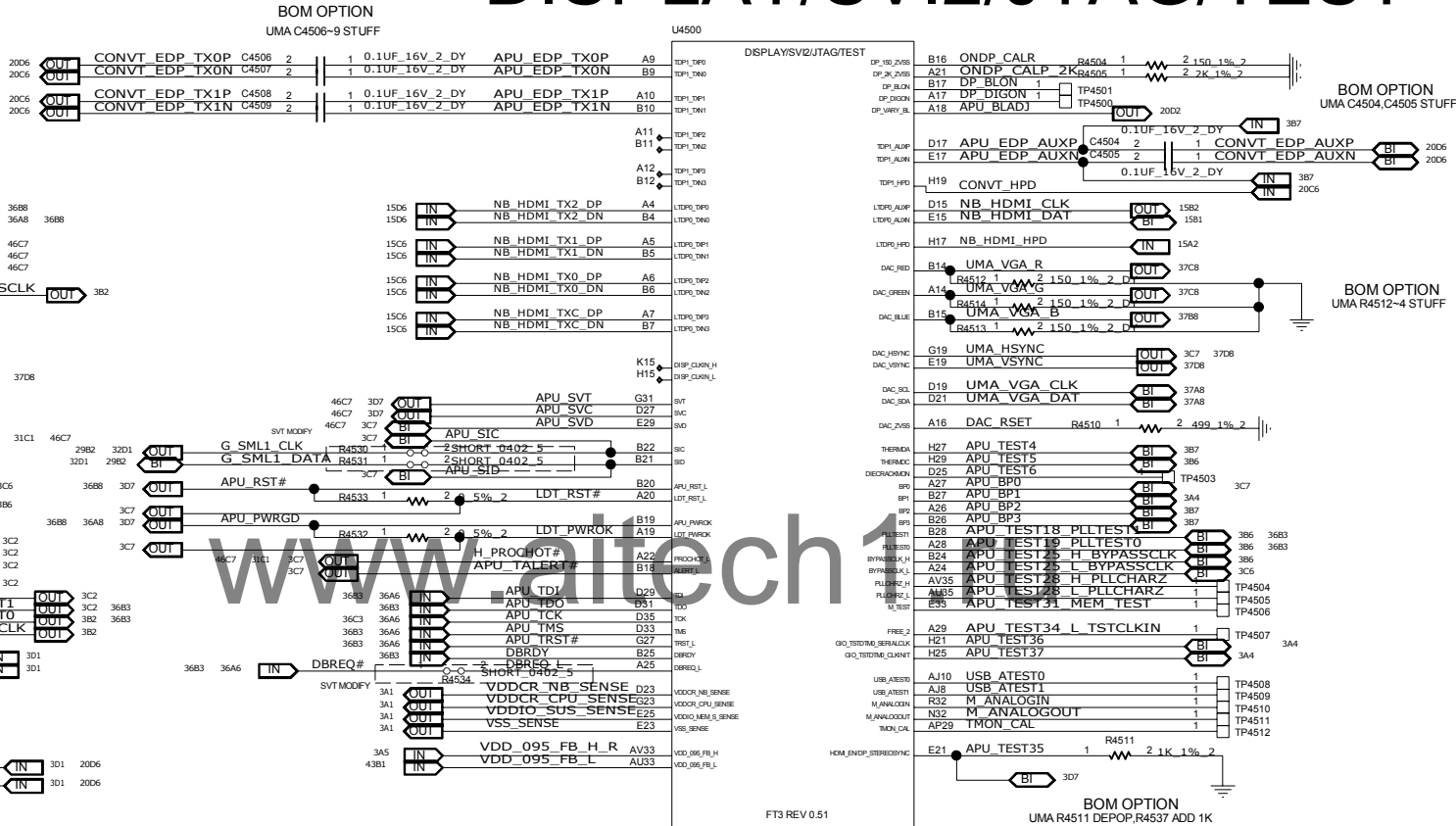
# KABINI BLOCK DIAGRAM



T&I			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by xxx DATE 21-OCT-2002 SHEET 2 of 55

# DISPLAY/SVI2/JTAG/TEST



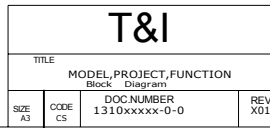
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TITLE <h2 style="margin: 0;">MODEL, PROJECT, FUNCTION</h2> <div style="display: flex; justify-content: space-around; margin-top: 5px;"> <span>Block</span> <span>Diagram</span> </div>			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET    3    of    55			

# ACPI/SD/AZ/GPIO/RTC/MISC

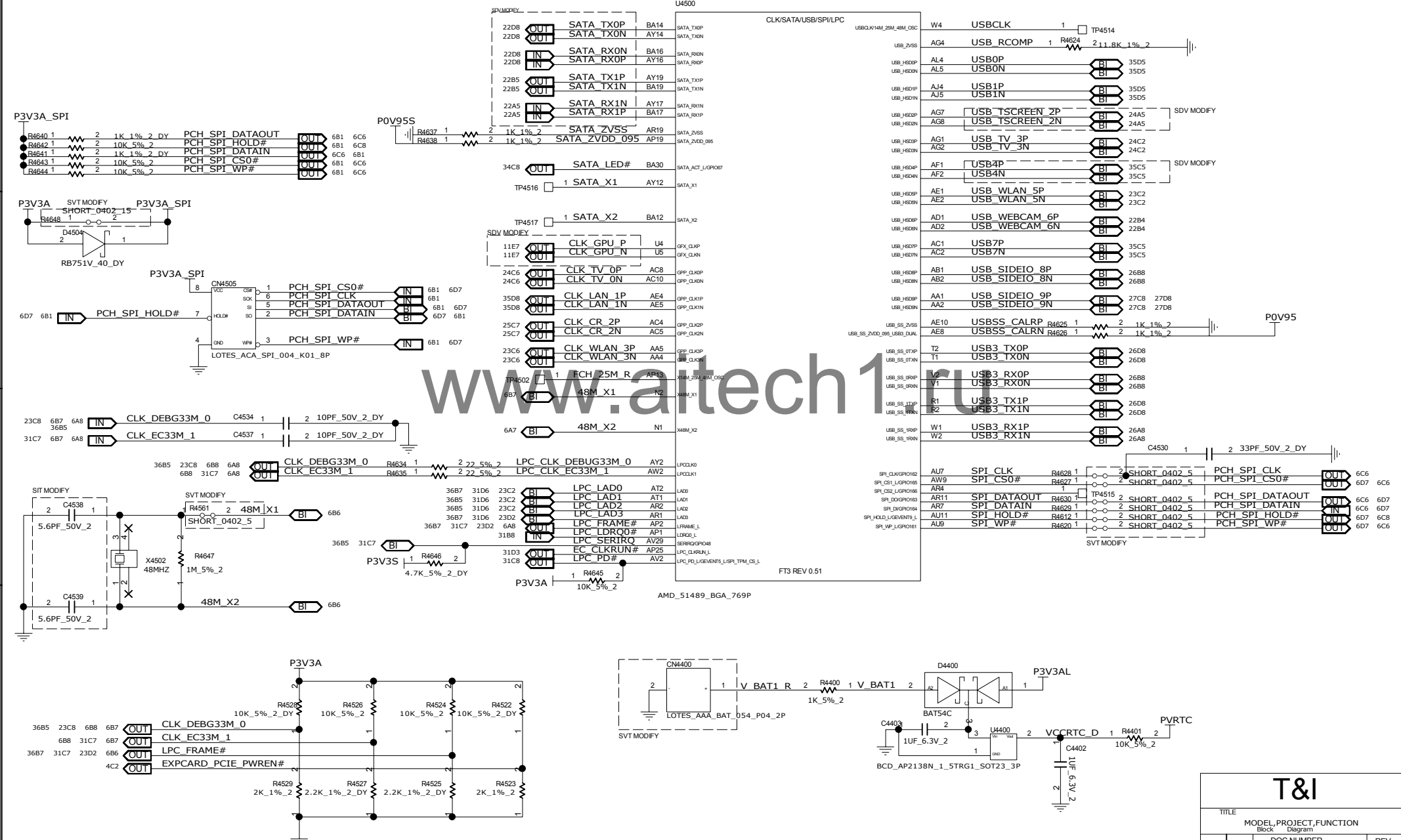
TITLE			
MODEL, PROJECT, FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 4 of 55			

CHANGE by	XXX	DATE	21-OCT-2002
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SD/MONEY U4500



# APU DDR/GND

D

C

B

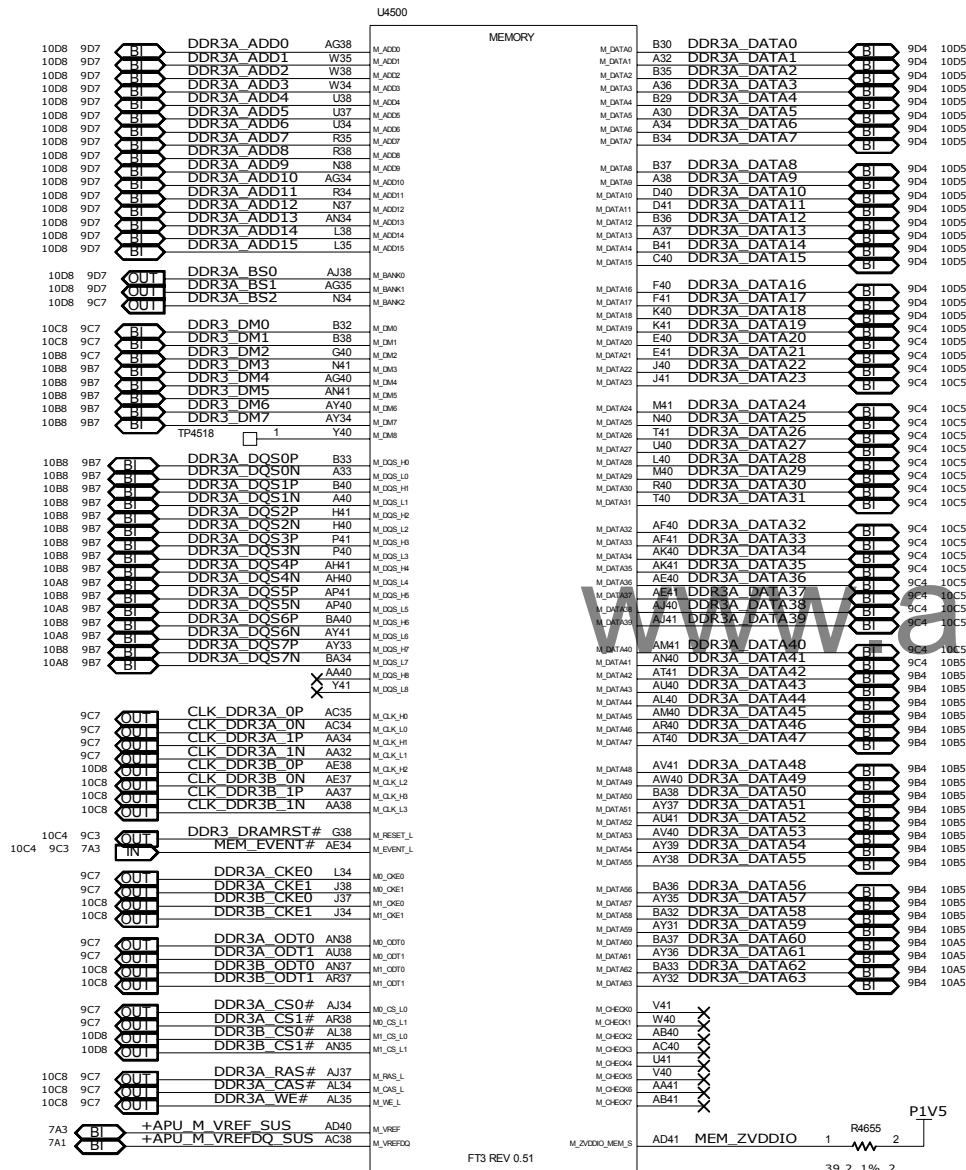
A

D

C

B

A

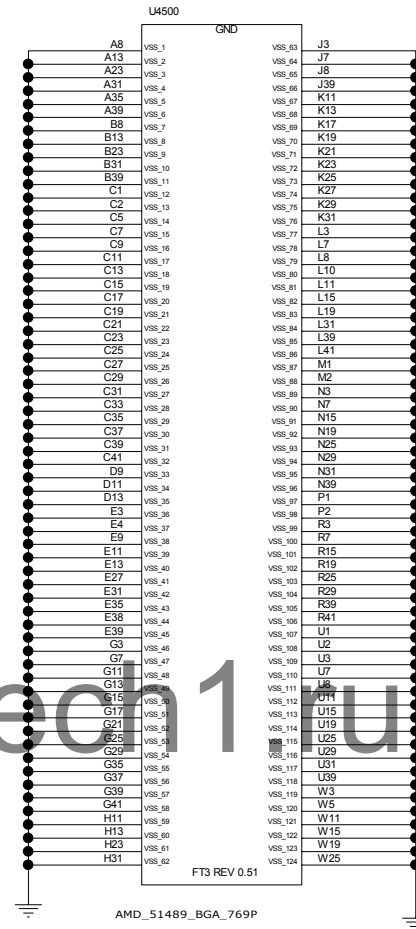


AMD\_51489\_BGA\_769P

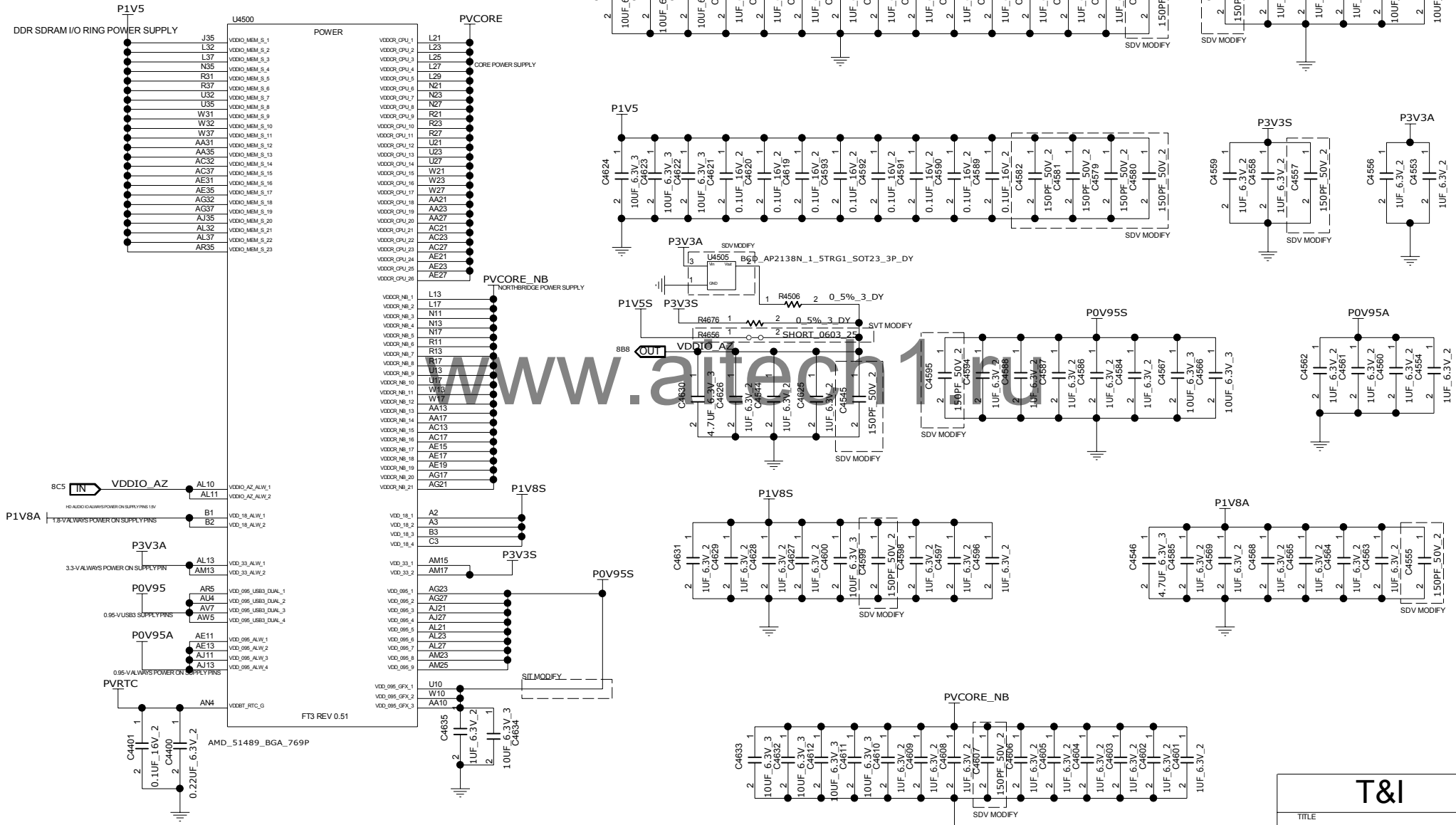
482 4A5 BI CPU\_MEMHOT# 3

482 4A5 BI CPU\_MEMHOT# 3

MEM\_EVENT# BI 9C3 10C4 7B8



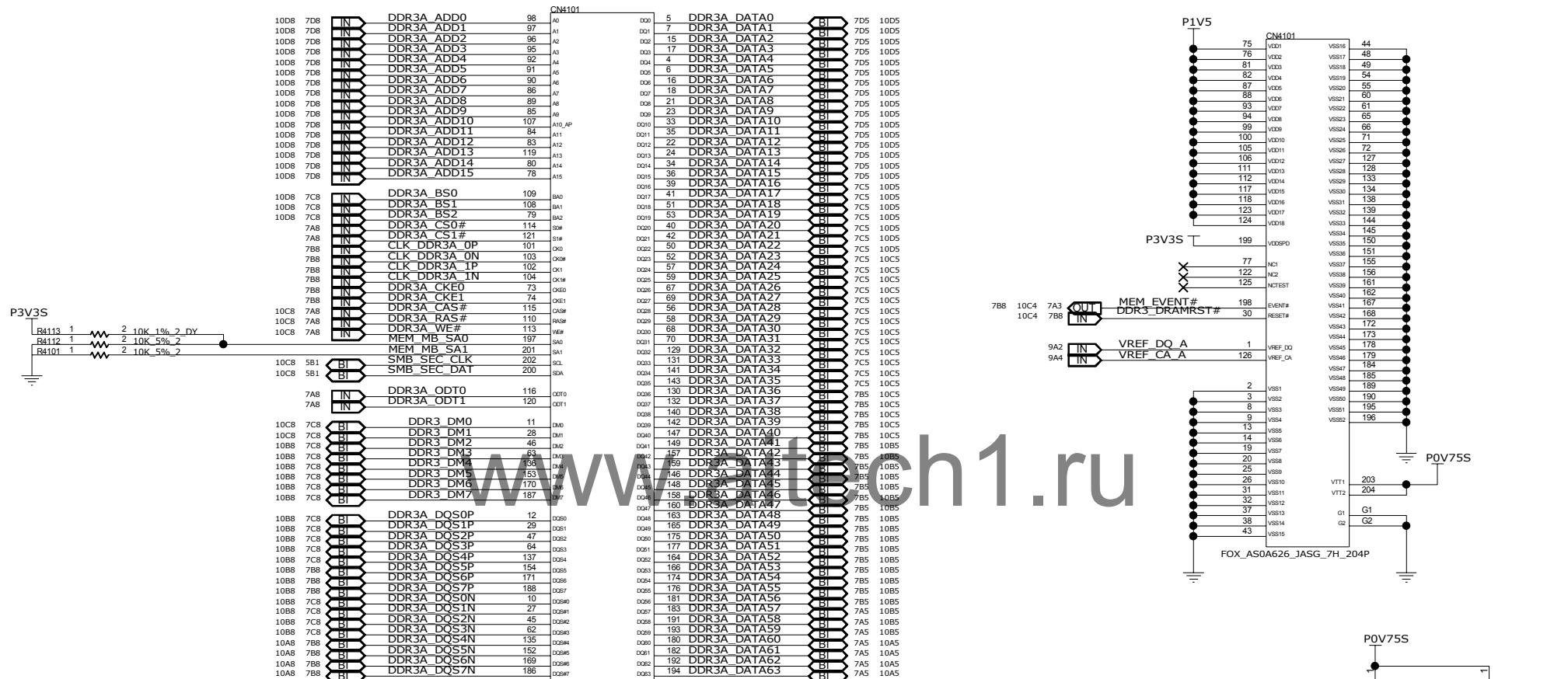
# APU POWER



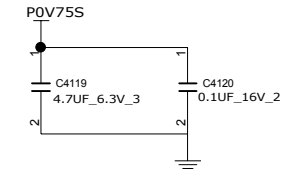
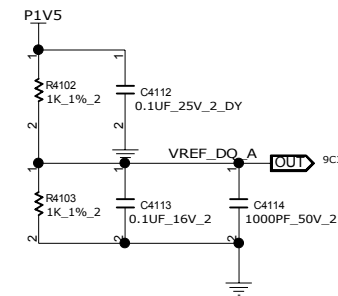
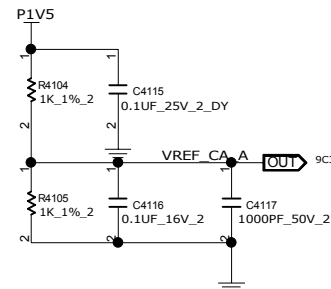
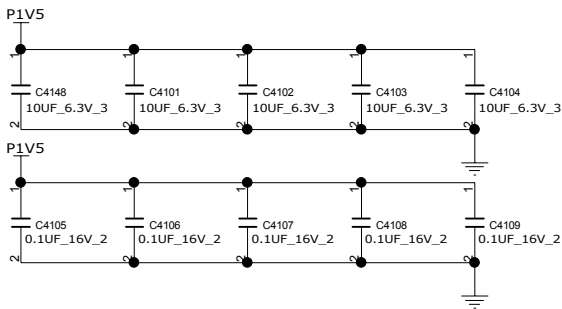
T&I			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
SHEET 8 of 55			



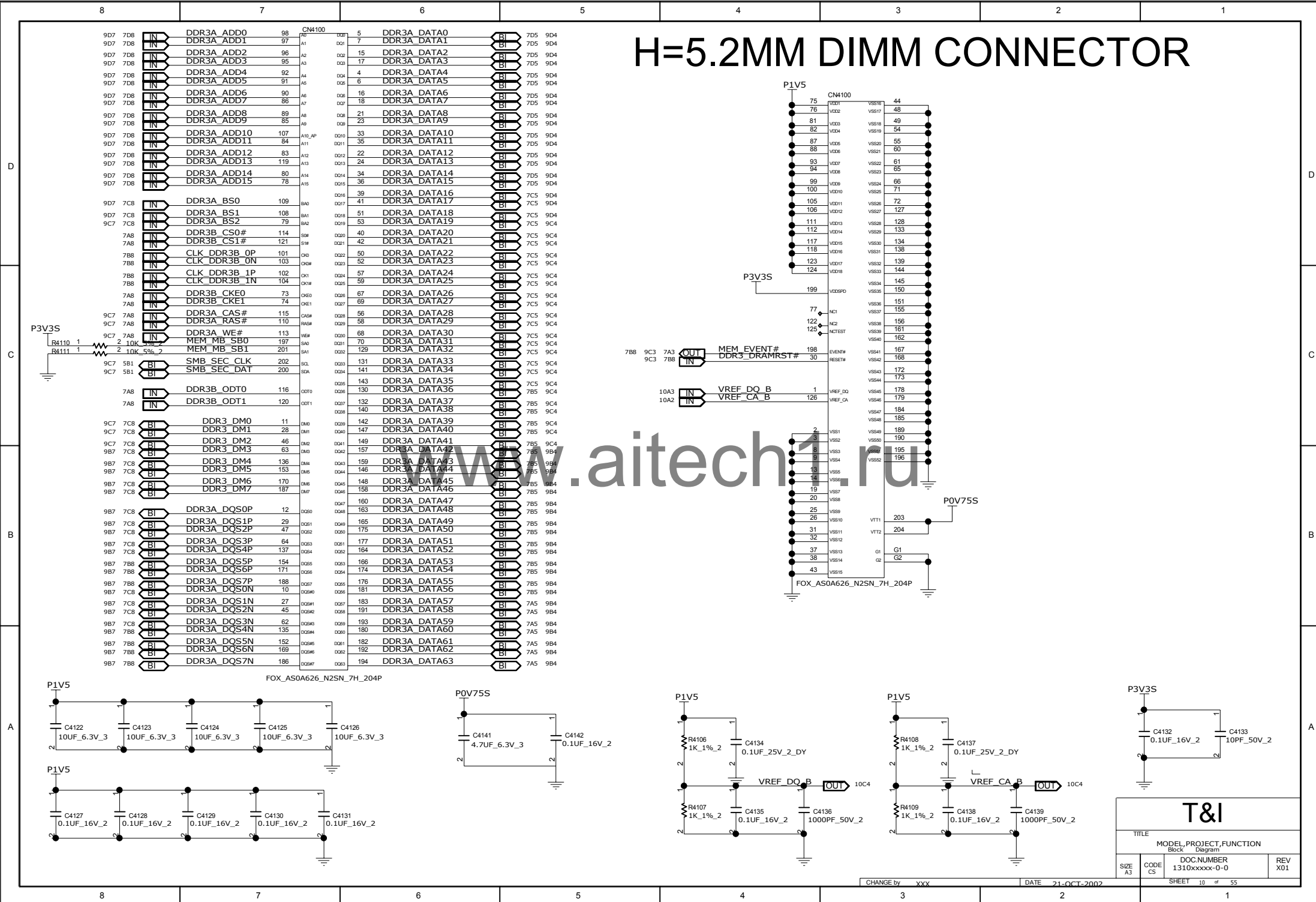
# H=9.2MM DIMM CONNECTOR



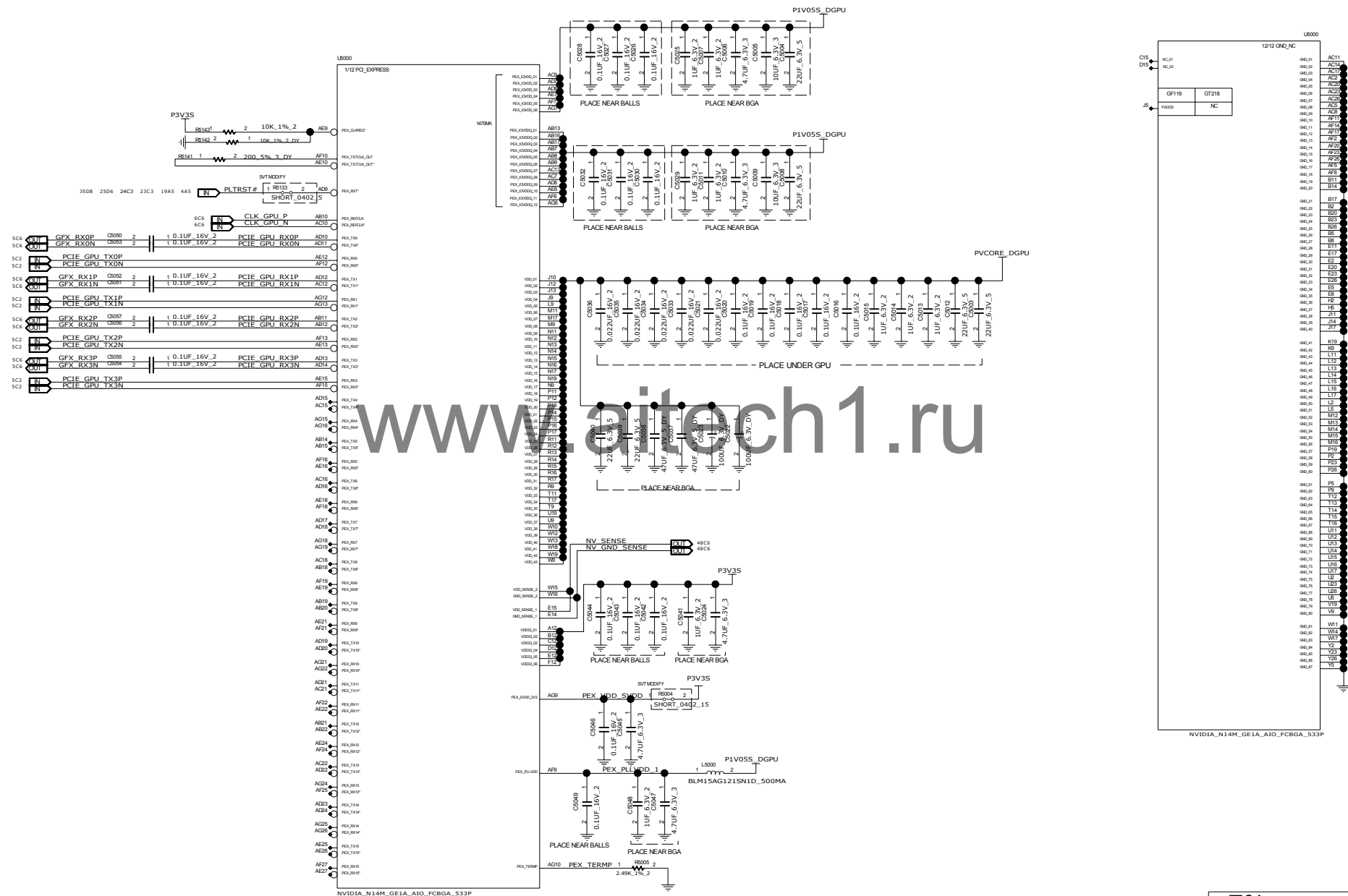
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T&I			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 9 of 55			



# GPU PCIE//POWER/GND



T&I
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TITLE	
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MODEL, PROJECT, FUNCTION  
Block Diagram

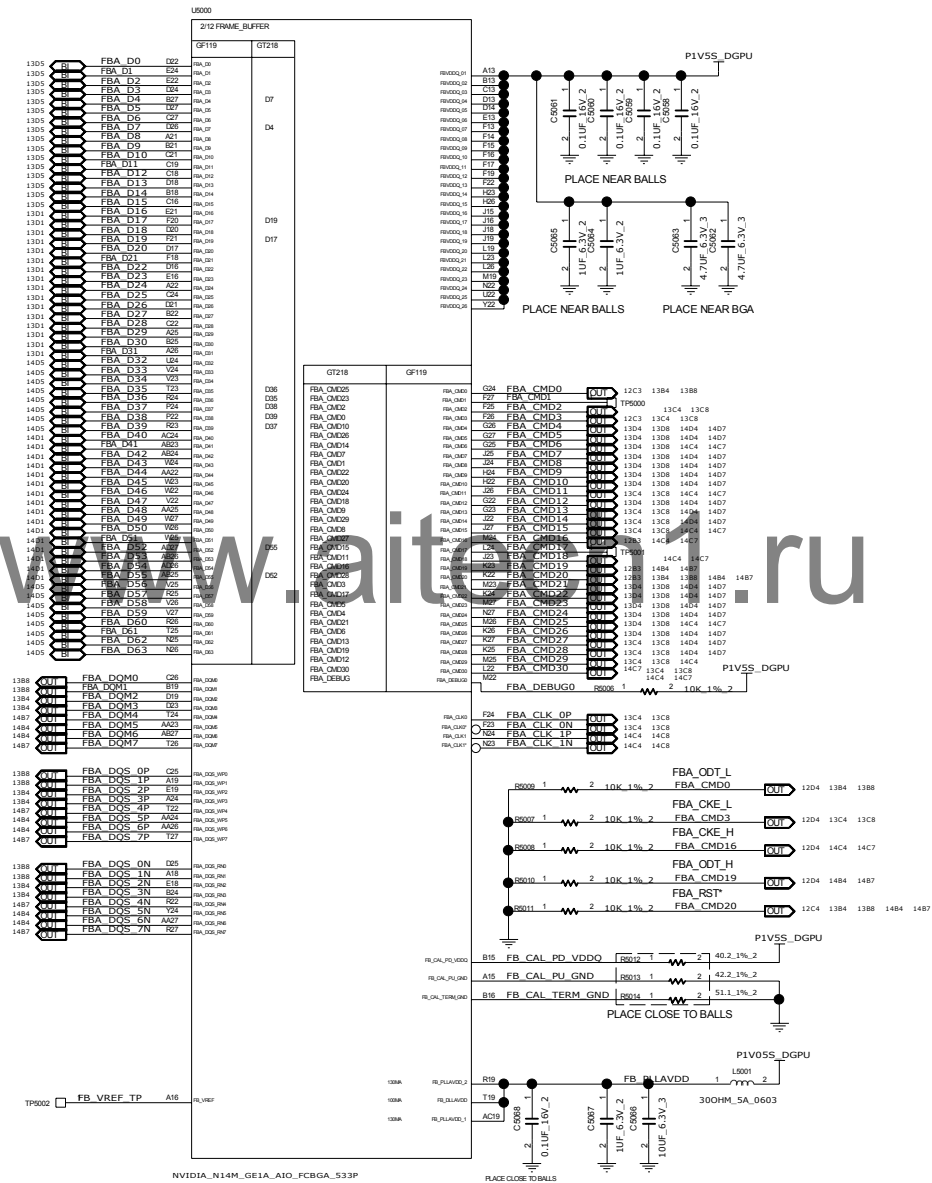
DATE	CODE	DOC NUMBER
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SIZE	CODE	DOC NUMBER
C	CS	1310xxxxx-0-0

CHANGE by	mmv	DATE	24 OCT 200
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# GPU DDR



The diagram illustrates the PCB layout for the VRAM LOWER 32 BIT, divided into two symmetrical halves (left and right). The layout includes various components, connectors, and a central watermark 'www.aitech1.ru'.

**Key Components and Connectors:**

- VRAM VREFDQ A H2** and **VRAM VREFCA A M9** (Top Left and Right)
- FBA CMD7 N4** through **FBA CMD30 M8** (Top Left and Right)
- FBA CMD29 M3**, **FBA CMD13 N9**, **FBA CMD27 M4** (Middle Left and Right)
- FBA CMD3 K10**, **FBA CLK 0P J8**, **FBA CLK 0N K8** (Middle Left and Right)
- FBA CMD11 J4**, **FBA CMD15 K4**, **FBA CMD28 L4**, **FBA CMD2 L3** (Middle Left and Right)
- FBA CMD20 T3**, **FBA CMD0 K2** (Bottom Left and Right)
- FBA DQS 0P F4**, **FBA DQS 1P C8**, **FBA DQM0 E8**, **FBA DQM1 D4**, **FBA DQS 0N G4**, **FBA DQS 1N B8** (Bottom Left and Right)
- FBA\_ZQ0 L9** and **FBA\_ZQ1 L9** (Bottom Left and Right)

**Connectors and Pins:**

- 13D4**, **13A7**, **13D4**, **13A4** (Top Left and Right)
- 14D7**, **14D4**, **13D4**, **12D4** (Top Left and Right)
- 14C7**, **14C4**, **13C4**, **12C4** (Top Left and Right)
- 14B7**, **14B4**, **13B4**, **12B4** (Bottom Left and Right)
- 12C6**, **12C6**, **12C6**, **12C6**, **12B6**, **12B6** (Bottom Left and Right)
- A1**, **A11**, **T1**, **T11**, **J2**, **J10**, **L2**, **L10** (Bottom Left and Right)

**Power and Grounding:**

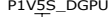
- P1V5S\_DGPU** (Power and Grounding)
- R5501**, **R5502**, **R5503**, **R5504**, **R5505**, **R5506** (Resistors)
- C5516**, **C5517**, **C5518**, **C5519**, **C5520**, **C5521**, **C5522**, **C5523**, **C5524**, **C5525**, **C5526**, **C5527**, **C5528**, **C5529**, **C5530**, **C5531**, **C5532**, **C5533**, **C5534**, **C5535**, **C5536**, **C5537**, **C5538**, **C5539**, **C5540**, **C5541**, **C5542**, **C5543**, **C5544**, **C5545**, **C5546**, **C5547**, **C5548**, **C5549**, **C5550**, **C5551**, **C5552**, **C5553**, **C5554**, **C5555**, **C5556**, **C5557**, **C5558**, **C5559**, **C5560**, **C5561**, **C5562**, **C5563**, **C5564**, **C5565**, **C5566**, **C5567**, **C5568**, **C5569**, **C5570**, **C5571**, **C5572**, **C5573**, **C5574**, **C5575**, **C5576**, **C5577**, **C5578**, **C5579**, **C5580**, **C5581**, **C5582**, **C5583**, **C5584**, **C5585**, **C5586**, **C5587**, **C5588**, **C5589**, **C5590**, **C5591**, **C5592**, **C5593**, **C5594**, **C5595**, **C5596**, **C5597**, **C5598**, **C5599**, **C5600**, **C5601**, **C5602**, **C5603**, **C5604**, **C5605**, **C5606**, **C5607**, **C5608**, **C5609**, **C5610**, **C5611**, **C5612**, **C5613**, **C5614**, **C5615**, **C5616**, **C5617**, **C5618**, **C5619**, **C5620**, **C5621**, **C5622**, **C5623**, **C5624**, **C5625**, **C5626**, **C5627**, **C5628**, **C5629**, **C5630**, **C5631**, **C5632**, **C5633**, **C5634**, **C5635**, **C5636**, **C5637**, **C5638**, **C5639**, **C5640**, **C5641**, **C5642**, **C5643**, **C5644**, **C5645**, **C5646**, **C5647**, **C5648**, **C5649**, **C5650**, **C5651**, **C5652**, **C5653**, **C5654**, **C5655**, **C5656**, **C5657**, **C5658**, **C5659**, **C5660**, **C5661**, **C5662**, **C5663**, **C5664**, **C5665**, **C5666**, **C5667**, **C5668**, **C5669**, **C5670**, **C5671**, **C5672**, **C5673**, **C5674**, **C5675**, **C5676**, **C5677**, **C5678**, **C5679**, **C5680**, **C5681**, **C5682**, **C5683**, **C5684**, **C5685**, **C5686**, **C5687**, **C5688**, **C5689**, **C5690**, **C5691**, **C5692**, **C5693**, **C5694**, **C5695**, **C5696**, **C5697**, **C5698**, **C5699**, **C5700**, **C5701**, **C5702**, **C5703**, **C5704**, **C5705**, **C5706**, **C5707**, **C5708**, **C5709**, **C5710**, **C5711**, **C5712**, **C5713**, **C5714**, **C5715**, **C5716**, **C5717**, **C5718**, **C5719**, **C5720**, **C5721**, **C5722**, **C5723**, **C5724**, **C5725**, **C5726**, **C5727**, **C5728**, **C5729**, **C5730**, **C5731**, **C5732**, **C5733**, **C5734**, **C5735**, **C5736**, **C5737**, **C5738**, **C5739**, **C5740**, **C5741**, **C5742**, **C5743**, **C5744**, **C5745**, **C5746**, **C5747**, **C5748**, **C5749**, **C5750**, **C5751**, **C5752**, **C5753**, **C5754**, **C5755**, **C5756**, **C5757**, **C5758**, **C5759**, **C5760**, **C5761**, **C5762**, **C5763**, **C5764**, **C5765**, **C5766**, **C5767**, **C5768**, **C5769**, **C5770**, **C5771**, **C5772**, **C5773**, **C5774**, **C5775**, **C5776**, **C5777**, **C5778**, **C5779**, **C5780**, **C5781**, **C5782**, **C5783**, **C5784**, **C5785**, **C5786**, **C5787**, **C5788**, **C5789**, **C5790**, **C5791**, **C5792**, **C5793**, **C5794**, **C5795**, **C5796**, **C5797**, **C5798**, **C5799**, **C5800**, **C5801**, **C5802**, **C5803**, **C5804**, **C5805**, **C5806**, **C5807**, **C5808**, **C5809**, **C5810**, **C5811**, **C5812**, **C5813**, **C5814**, **C5815**, **C5816**, **C5817**, **C5818**, **C5819**, **C5820**, **C5821**, **C5822**, **C5823**, **C5824**, **C5825**, **C5826**, **C5827**, **C5**

TITLE		
MODEL,PROJECT,FUNCTION Block Diagram		
SIZE	CODE	DOC.NUMBER 1310xxxxx-0-0

DATE	21-OCT-2002
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SHEET 13 of 55

BOM OPTION GPU ONLY

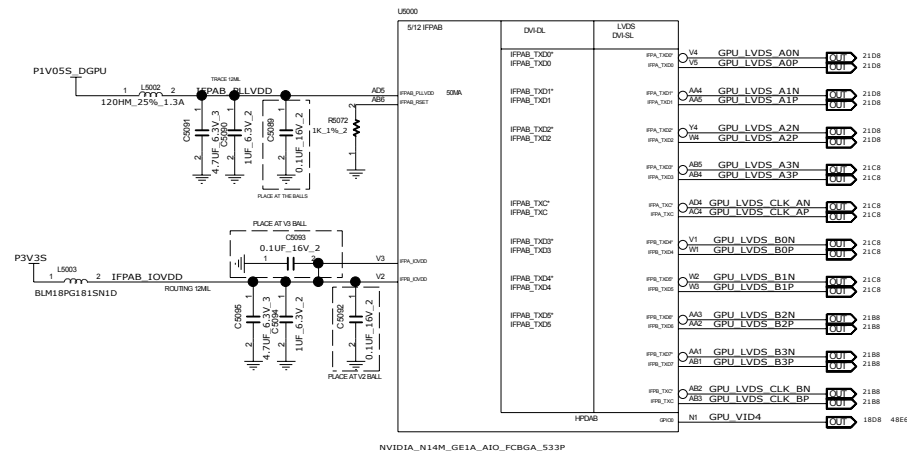


A3	CS	
SHEET 14 of 55		

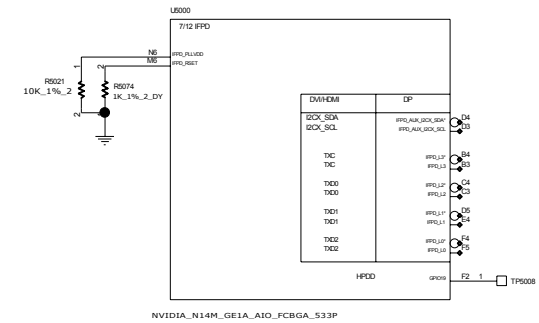
DATE	21-OCT-2002
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SHEET 14 of 55

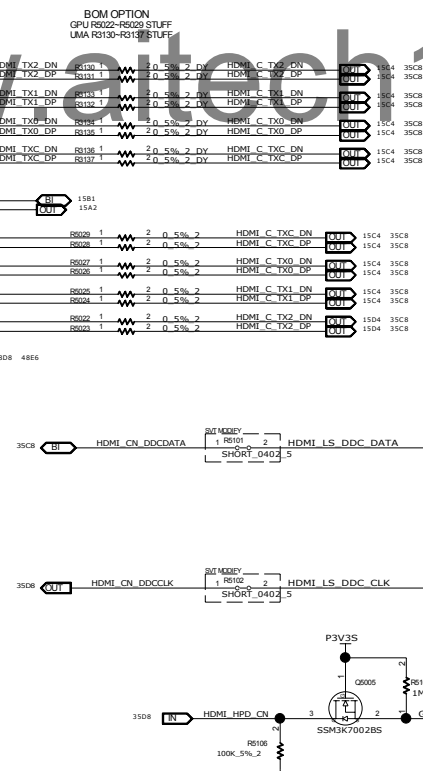
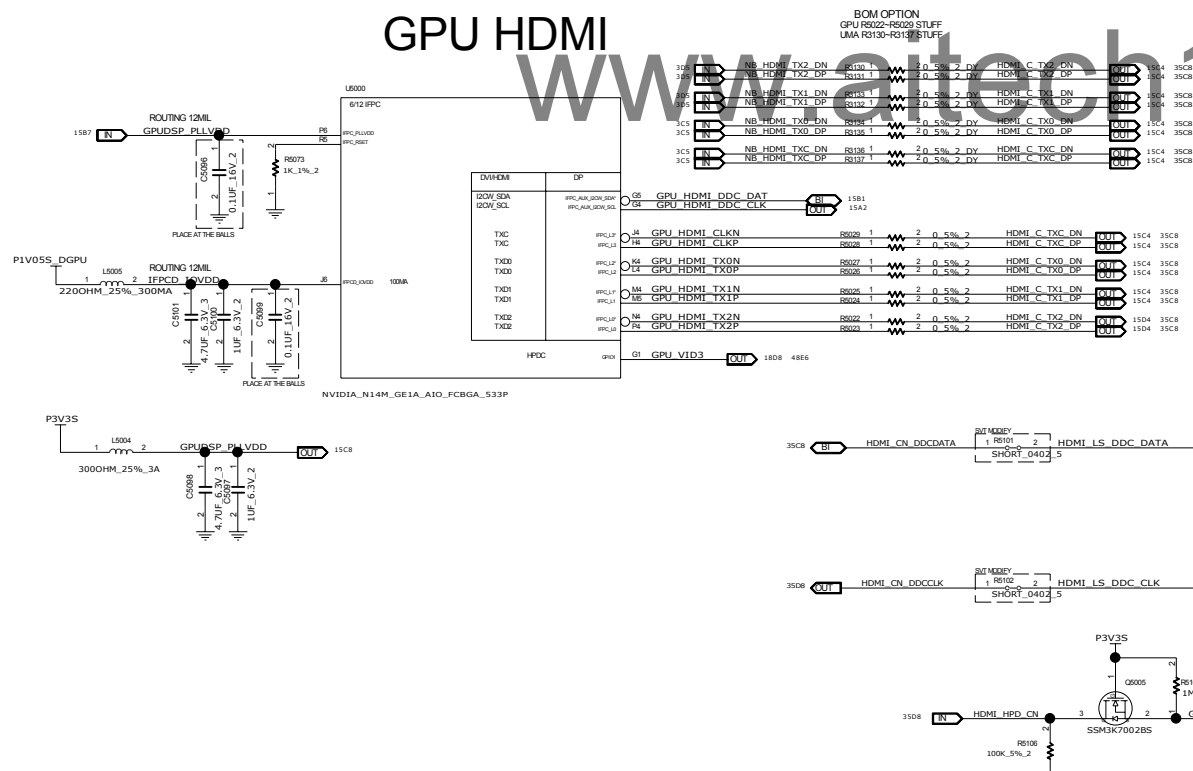
# GPU LVDS



# GPU DP

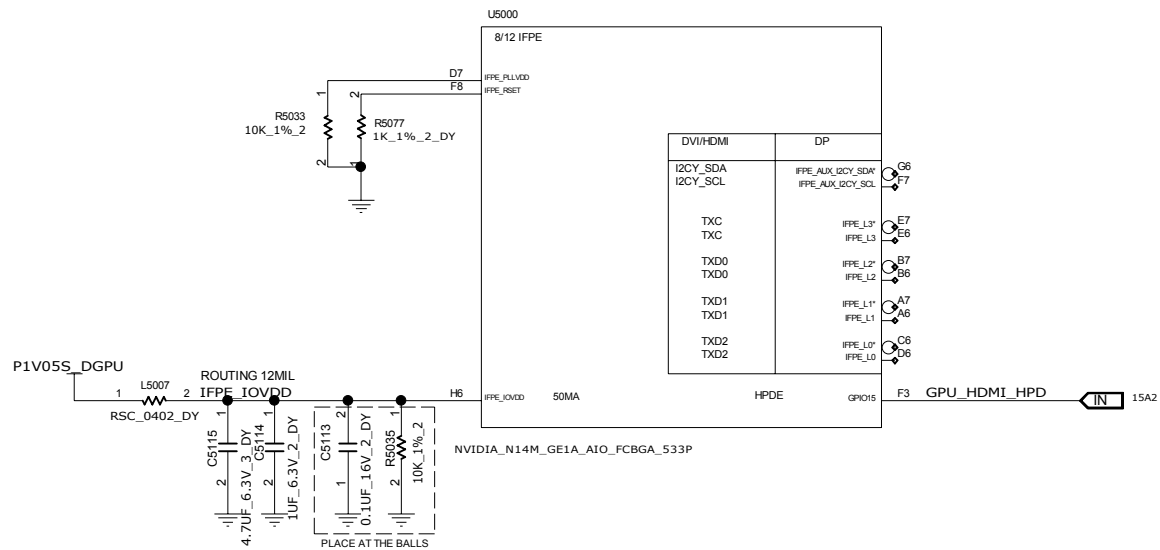


# GPU HDMI



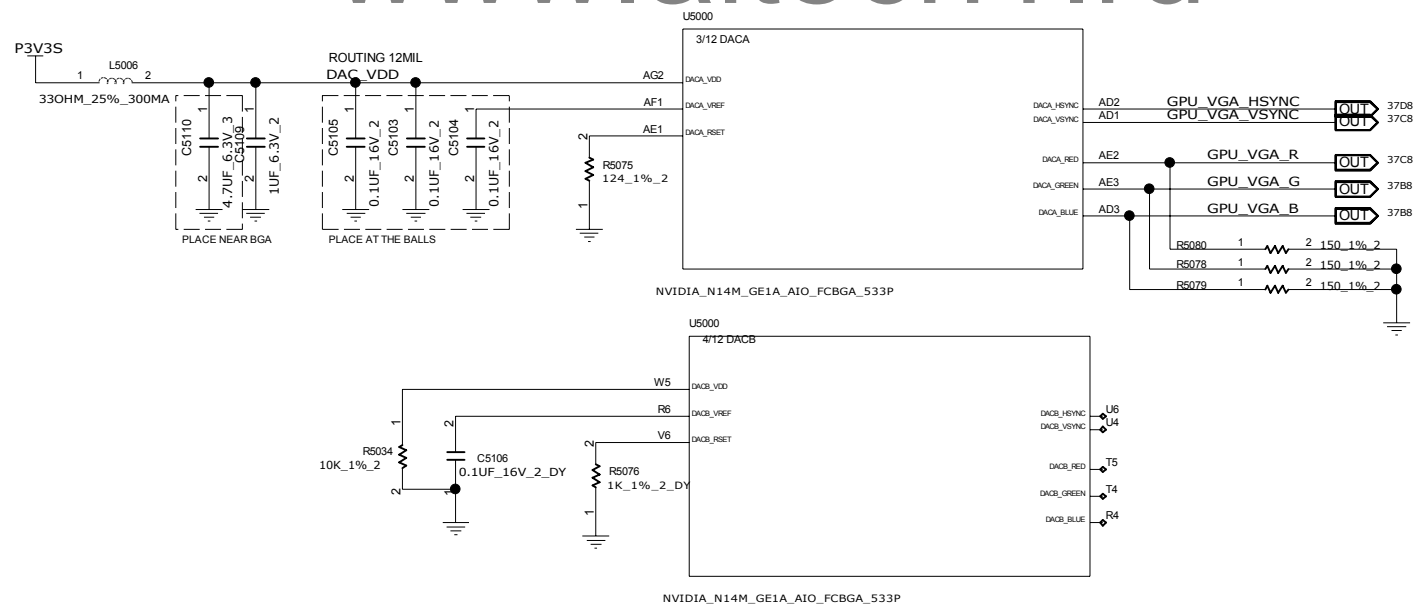
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MODEL, PROJECT, FUNCTION			
Block Diagram			
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1310XXXXXX-0-0	1310XXXXXX-0-0	1310XXXXXX-0-0	1310XXXXXX-0-0

# GPU DVI



# GPU VGA

GPU VGA

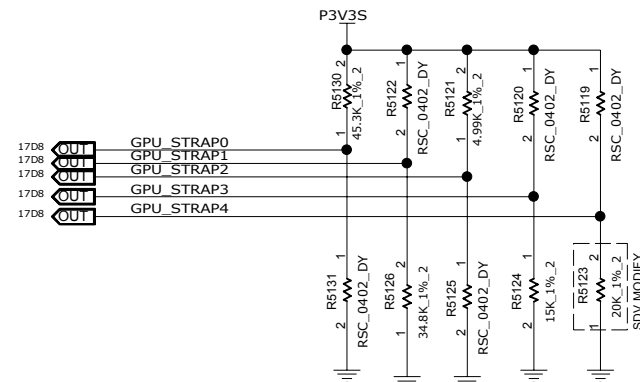


# INVENTEC

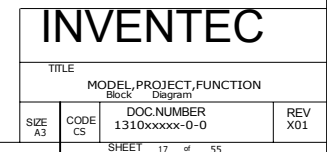
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MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE #2	CODE _CS	DOC.NUMBER 1310xxxxx-0-0		REV X01



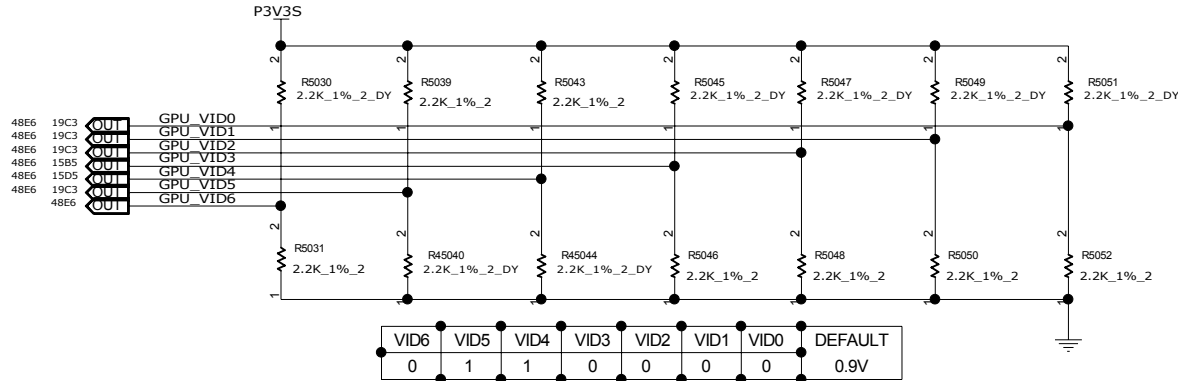
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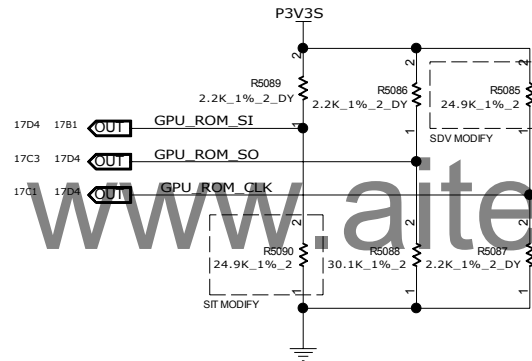
## A



# GPU STRAPING / VID



Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111



GPU_ROM_SI	VRAM SKU TABLE
R5090	VRAM SKU TABLE
15K	H5TQ1G63DFR-11C PN:6019B0873101 HYNIX 64MX16:512M
20K	K4W1G1646G-BC11 PN:6W19A0026901 SAMSUNG 64MX16:512M
24.9K	H5TQ2G63DFR-11C PN: 6019B0973101(OLD) HYNIX128MX16: 1G
15K	H5TC2G63FFR-11C PN:6019B1088301(NEW)
4.99K	K4W2G1646E-HC11 PN: 6019B0986201 SAMSUNG 128MX16:1G

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

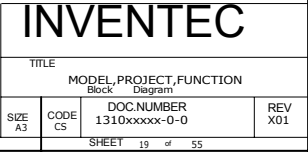
INVENTEC

TITLE			
MODEL_PROJECT_FUNCTION			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

CHANGE by xxx DATE 21-OCT-2002

SHEET 18 of 55

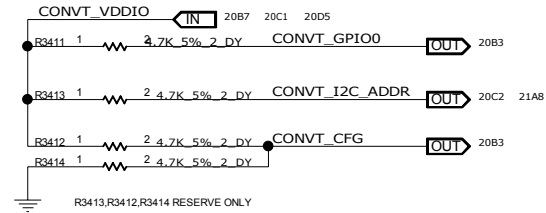
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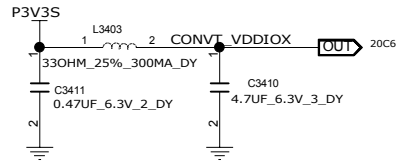
# PS8625

BOM OPTION UMA ONLY

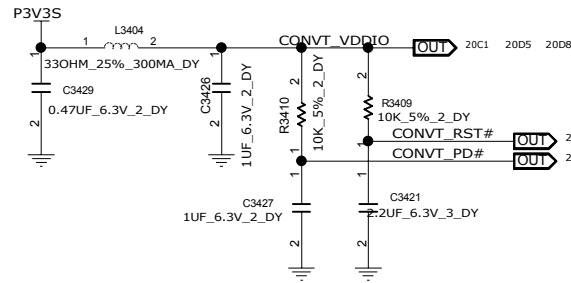
D



C

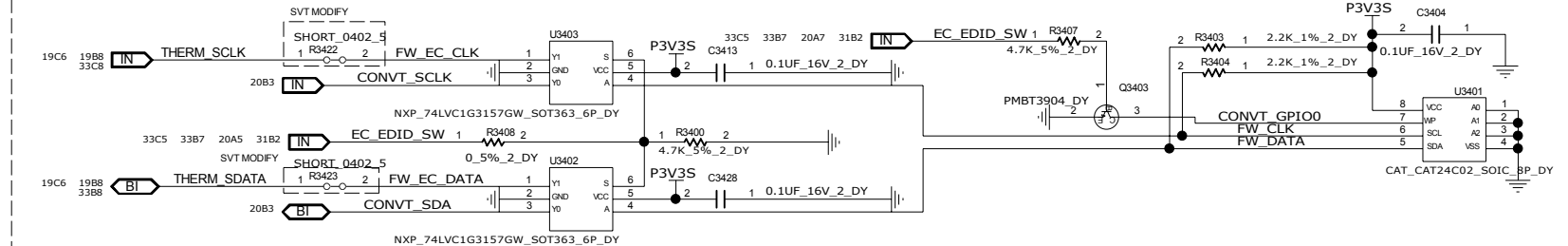


B

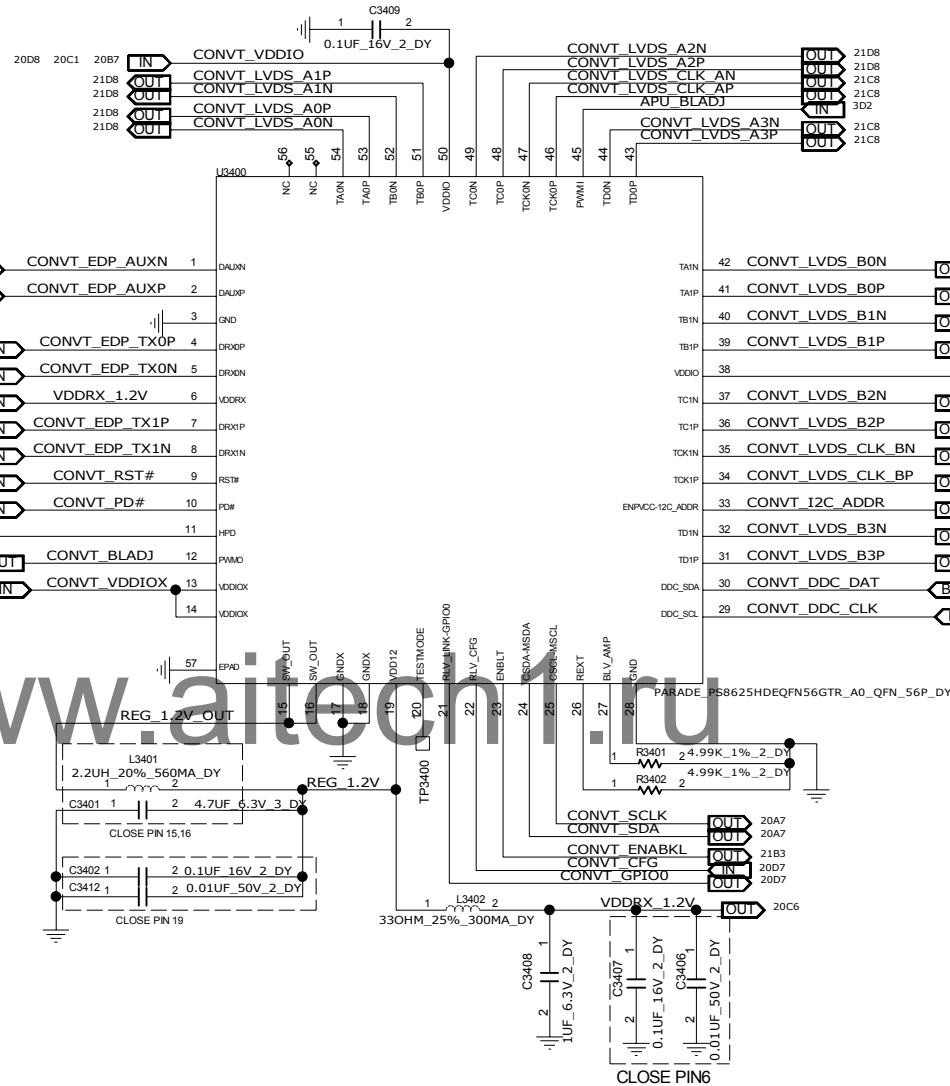


A

SDV MODIFY



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## INVENTEC

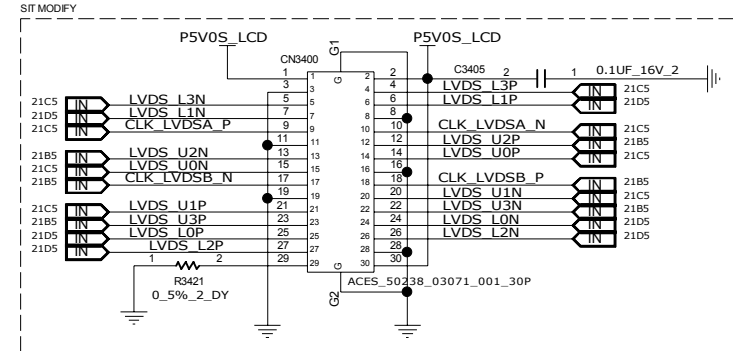
TITLE				
MODEL_PROJECT_FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET		20 of 55		

CHANGE by XXX DATE 21-OCT-2002

# LVDS CONNECTOR

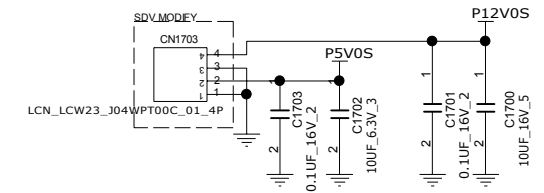
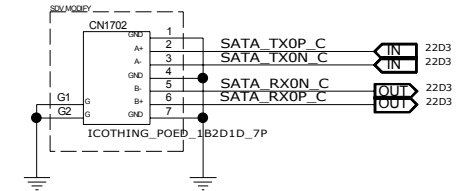
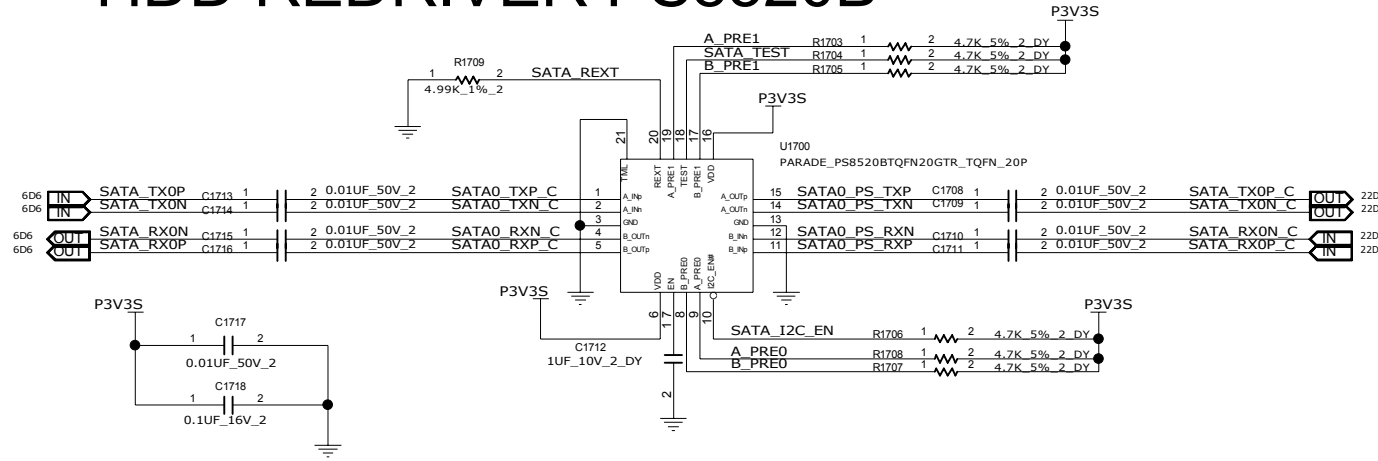
## BOM OPTION

15F5	IN	GPU LVDS A0P	R3434	1	2	0.5%	2	LVDS L0P	OUT	21D4
15F5	IN	GPU LVDS A0N	R3433	1	2	0.5%	2	LVDS L0N	OUT	21D1
2005	IN	CONVT LVDS A0P	R3432	1	2	0.5%	2_DY			
2005	IN	CONVT LVDS A0N	R3435	1	2	0.5%	2_DY			
15F5	IN	GPU LVDS A1P	R3428	1	2	0.5%	2	LVDS L1P	OUT	21D1
15F5	IN	GPU LVDS A1N	R3426	1	2	0.5%	2	LVDS L1N	OUT	21D4
2005	IN	CONVT LVDS A1P	R3425	1	2	0.5%	2_DY			
2005	IN	CONVT LVDS A1N	R3430	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS A2P	R3464	1	2	0.5%	2	LVDS L2P	OUT	21D4
15F5	IN	GPU LVDS A2N	R3448	1	2	0.5%	2	LVDS L2N	OUT	21D1
2002	IN	CONVT LVDS A2P	R3447	1	2	0.5%	2_DY			
2002	IN	CONVT LVDS A2N	R3452	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS A3P	R3446	1	2	0.5%	2	LVDS L3P	OUT	21D1
15E5	IN	GPU LVDS A3N	R3445	1	2	0.5%	2	LVDS L3N	OUT	21D4
2002	IN	CONVT LVDS A3P	R3436	1	2	0.5%	2_DY			
2002	IN	CONVT LVDS A3N	R3477	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS CLK AP	R3476	1	2	0.5%	2	CLK LVDSA P	OUT	21D4
15E5	IN	GPU LVDS CLK AN	R3473	1	2	0.5%	2	CLK LVDSA N	OUT	21D1
2002	IN	CONVT LVDS CLK AP	R3467	1	2	0.5%	2_DY			
2002	IN	CONVT LVDS CLK AN	R3478	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS B0P	R3466	1	2	0.5%	2	LVDS U0P	OUT	21D1
15E5	IN	GPU LVDS B0N	R3465	1	2	0.5%	2	LVDS U0N	OUT	21D4
2002	IN	CONVT LVDS B0P	R3480	1	2	0.5%	2_DY			
2002	IN	CONVT LVDS B0N	R3488	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS B1P	R3486	1	2	0.5%	2	LVDS U1P	OUT	21D1
15E5	IN	GPU LVDS B1N	R3485	1	2	0.5%	2	LVDS U1N	OUT	21D1
2002	IN	CONVT LVDS B1P	R3484	1	2	0.5%	2_DY			
2002	IN	CONVT LVDS B1N	R3487	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS B2P	R3415	1	2	0.5%	2	LVDS U2P	OUT	21D1
15E5	IN	GPU LVDS B2N	R3416	1	2	0.5%	2	LVDS U2N	OUT	21D4
20C2	IN	CONVT LVDS B2P	R3417	1	2	0.5%	2_DY			
20C2	IN	CONVT LVDS B2N	R3418	1	2	0.5%	2_DY			
15E5	IN	GPU LVDS B3P	R3419	1	2	0.5%	2	LVDS U3P	OUT	21D4
15E5	IN	GPU LVDS B3N	R3420	1	2	0.5%	2	LVDS U3N	OUT	21D1
20C2	IN	CONVT LVDS B3P	R3491	1	2	0.5%	2_DY			
20C2	IN	CONVT LVDS B3N	R3490	1	2	0.5%	2_DY			
15D5	IN	GPU LVDS CLK BP	R3492	1	2	0.5%	2	CLK LVDSB P	OUT	21D1
15D5	IN	GPU LVDS CLK BN	R3495	1	2	0.5%	2	CLK LVDSB N	OUT	21D4
20C2	IN	CONVT LVDS CLK BP	R3496	1	2	0.5%	2_DY			
20C2	IN	CONVT LVDS CLK BN	R3497	1	2	0.5%	2_DY			



# HDD REDRIVER PS8520B

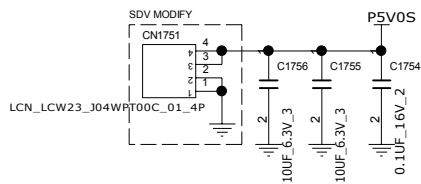
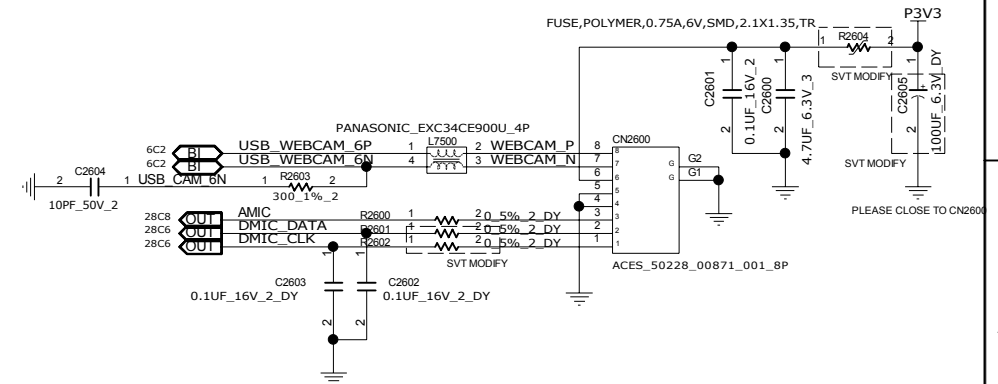
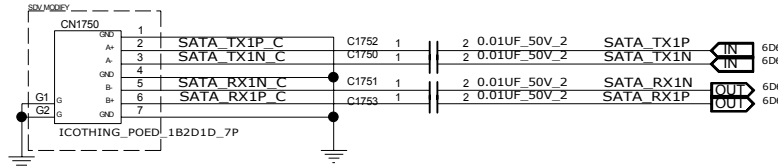
# HDD CONNECTOR



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# ODD CONNECTOR

# WEBCAM

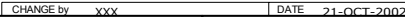


T&I				
TITLE				
MODEL PROJECT FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	

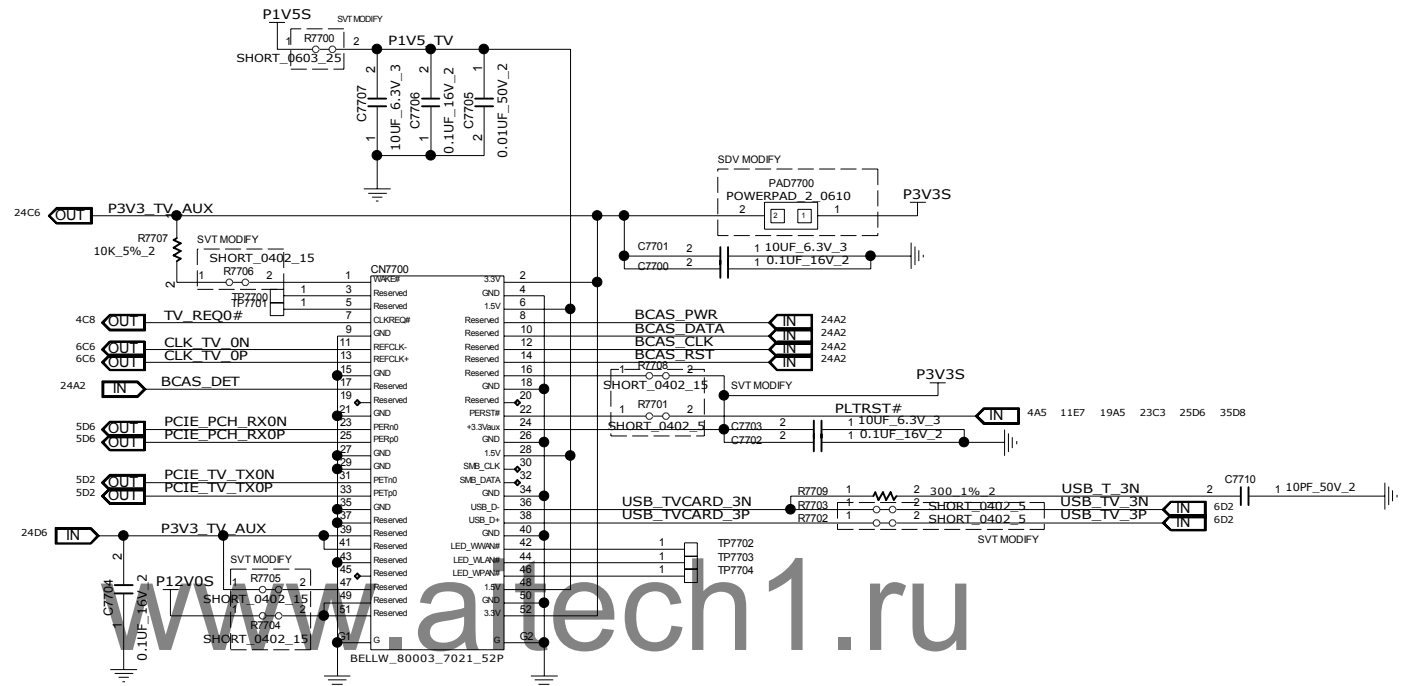
CHANGE by XXX DATE 21-OCT-2002

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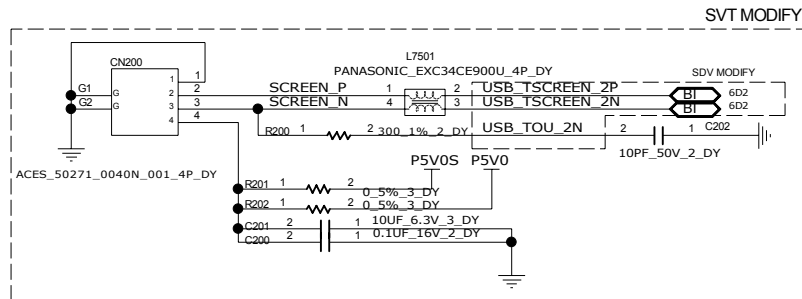
## A



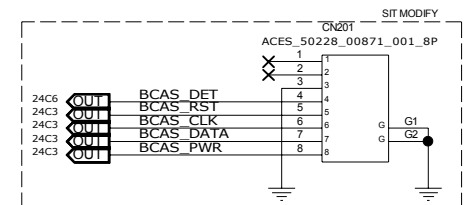
# MINI PCI-E TV CARD



# TOUCH SCREEN



# BCAS



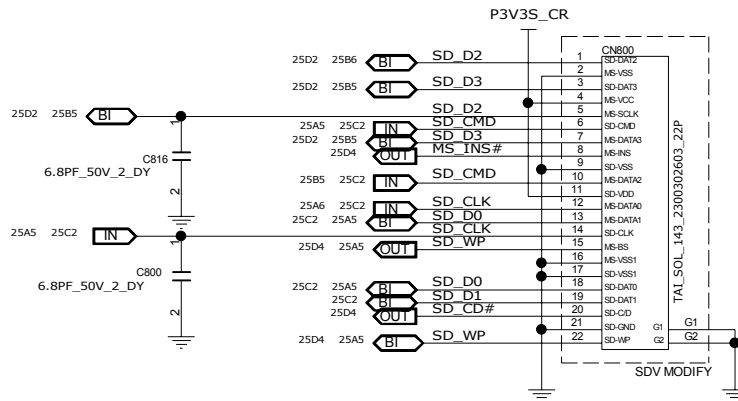
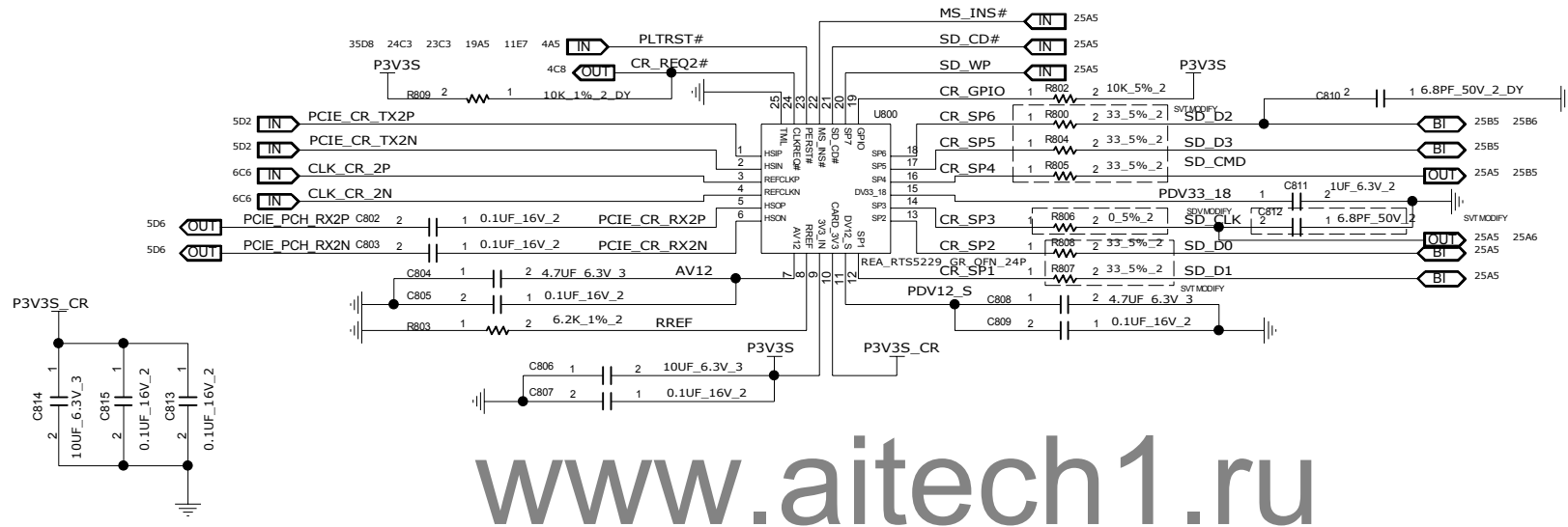
T&I

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

CHANGE by xxx DATE 21-OCT-2002 SHEET 24 of 55



# CARD READER RTS5229



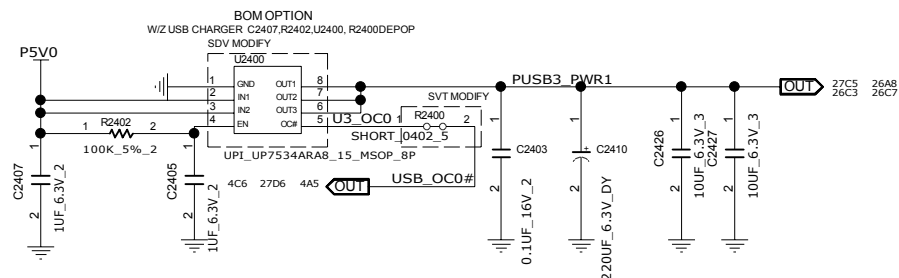
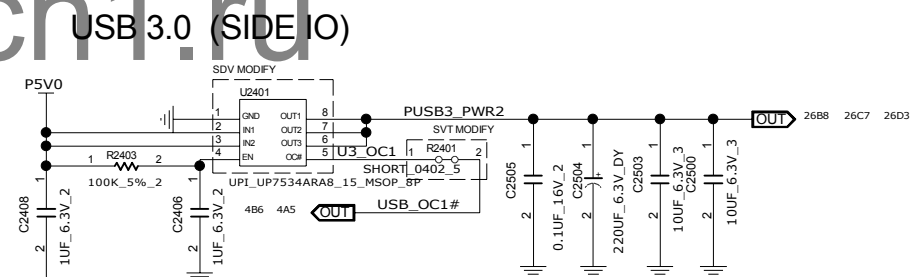
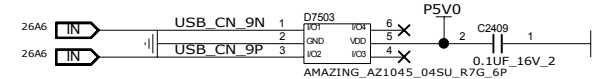
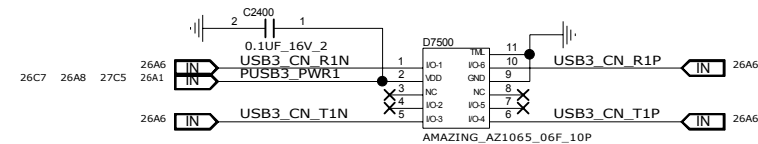
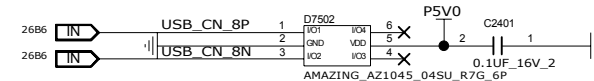
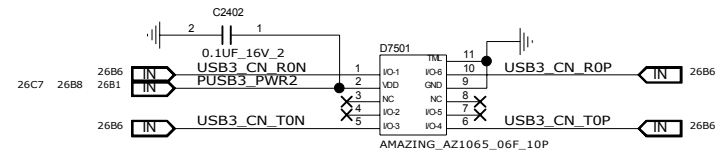
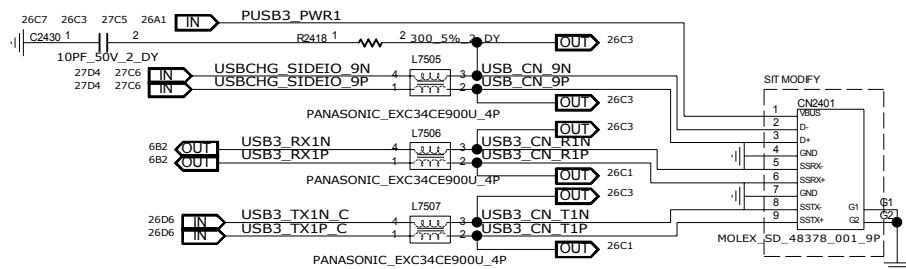
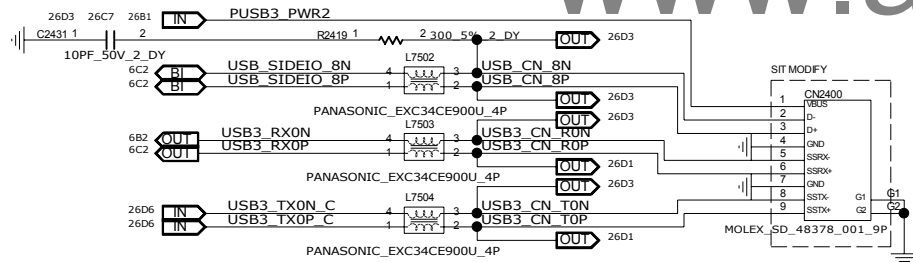
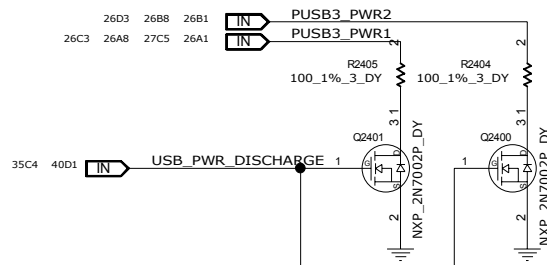
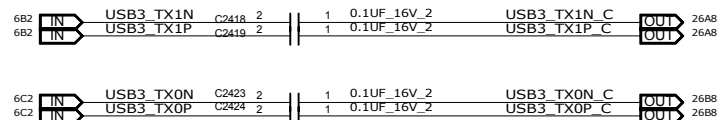
T&I

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

CHANGE by xxx DATE 21-OCT-2002

SHEET 25 of 55

# USB 3.0



T&I			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOCNUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by xxx DATE 21-OCT-2002 SHEET 26 of 55

8 7 6 5

BOM OPTION  
WIZ USB CHARGER R2509-11 DEPOP

USB CHA

7C8 6C2 IN USB\_SIDEIO\_9N 1 R2509 2 0 5% 2 USBCHG\_SIDEIO\_9N\_R 1 R2510 2 0 5% 2 USBCHG\_SIDEIO\_9N OUT 27C6 26A8  
7C8 6C2 IN USB\_SIDEIO\_9P 1 2 0 5% 2 USBCHG\_SIDEIO\_9P\_R 1 2 0 5% 2 USBCHG\_SIDEIO\_9P OUT 27C6 26A8

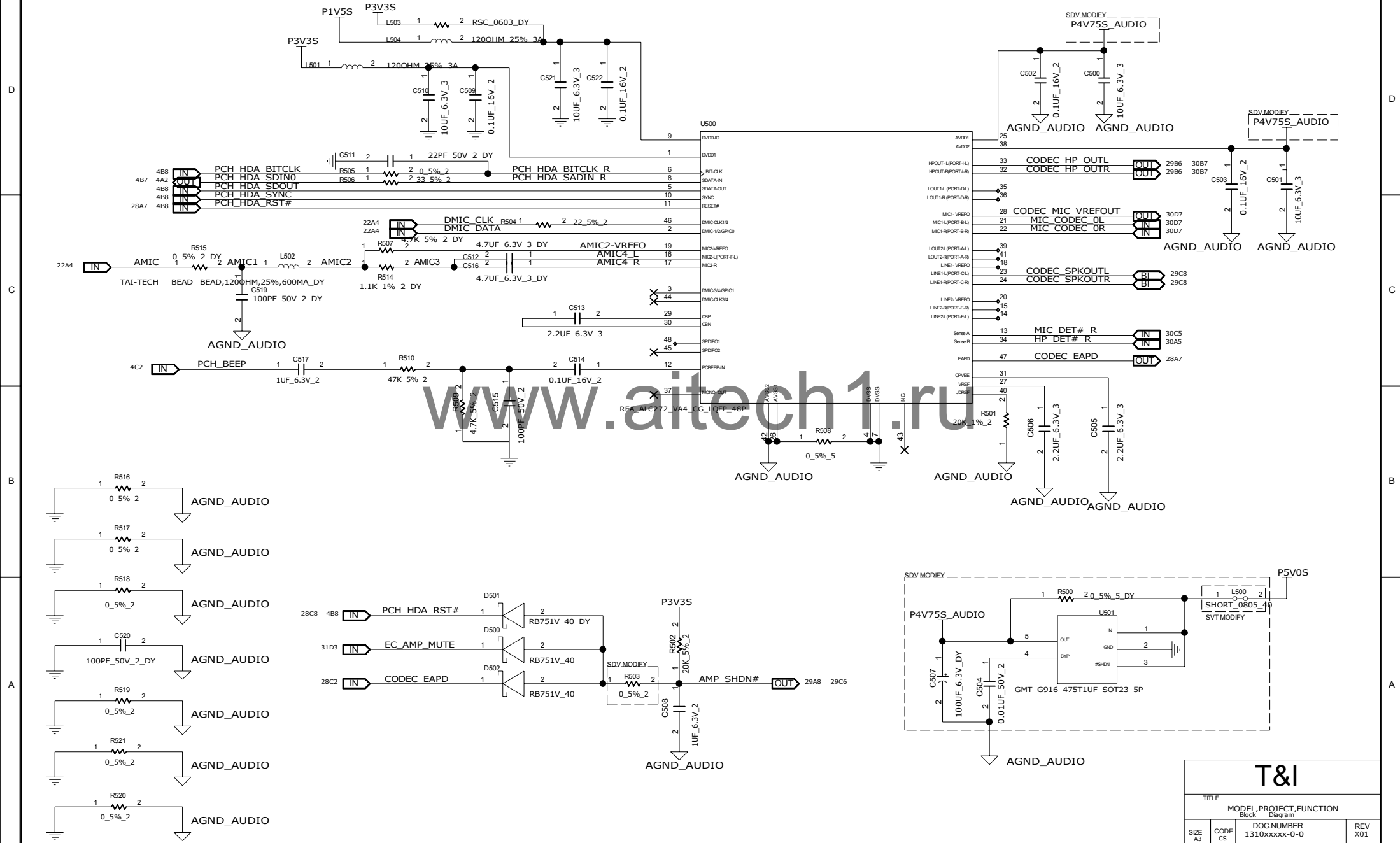
R2508 R2511



CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
5A	OFF	

BA

# AUDIO CODEC ALC272



T&I

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by xxx DATE 21-OCT-2002

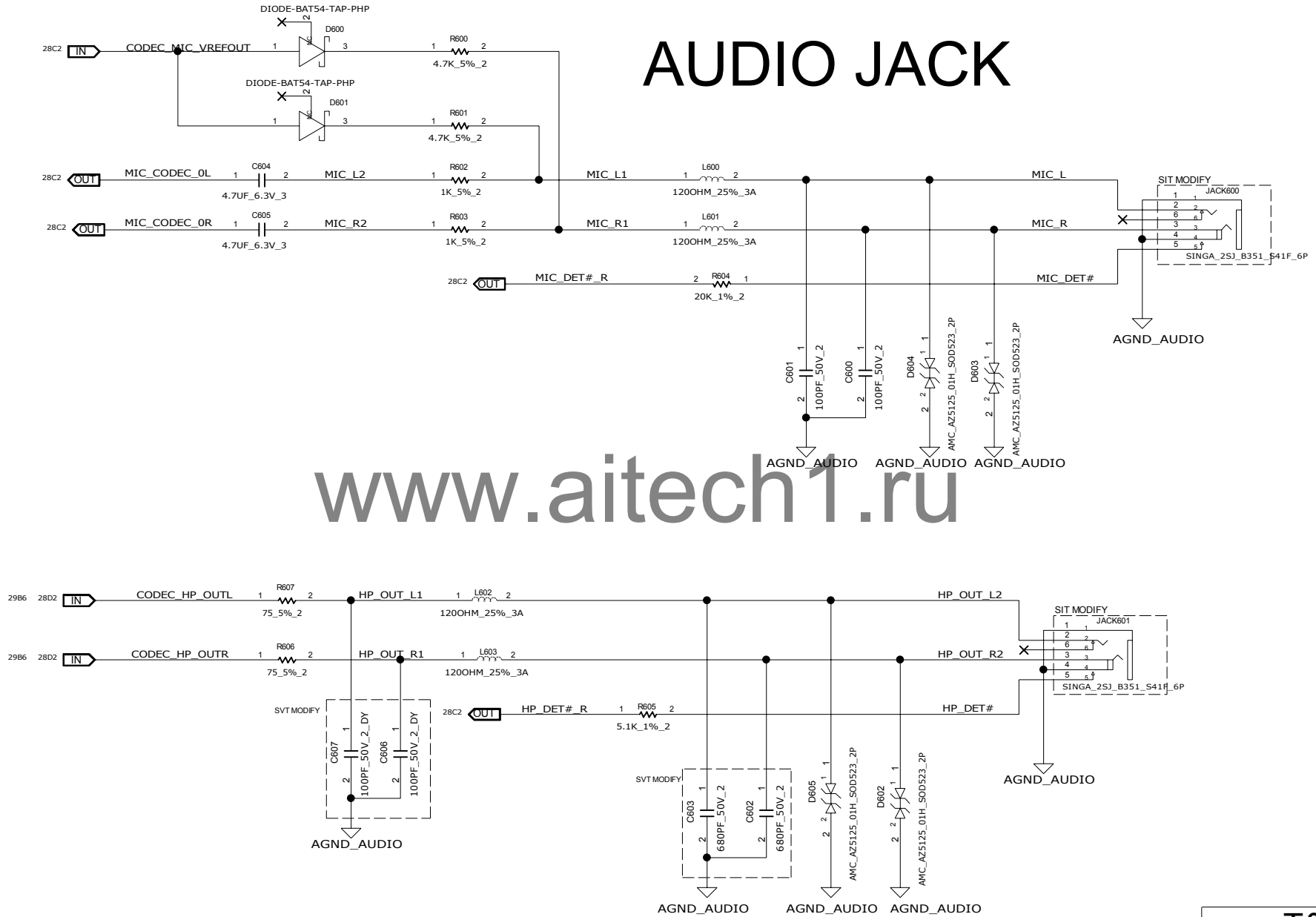
SHEET 28 of 55

## A



T&I			
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	REV X01
SHEET 70 of 75			

# AUDIO JACK



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T&I

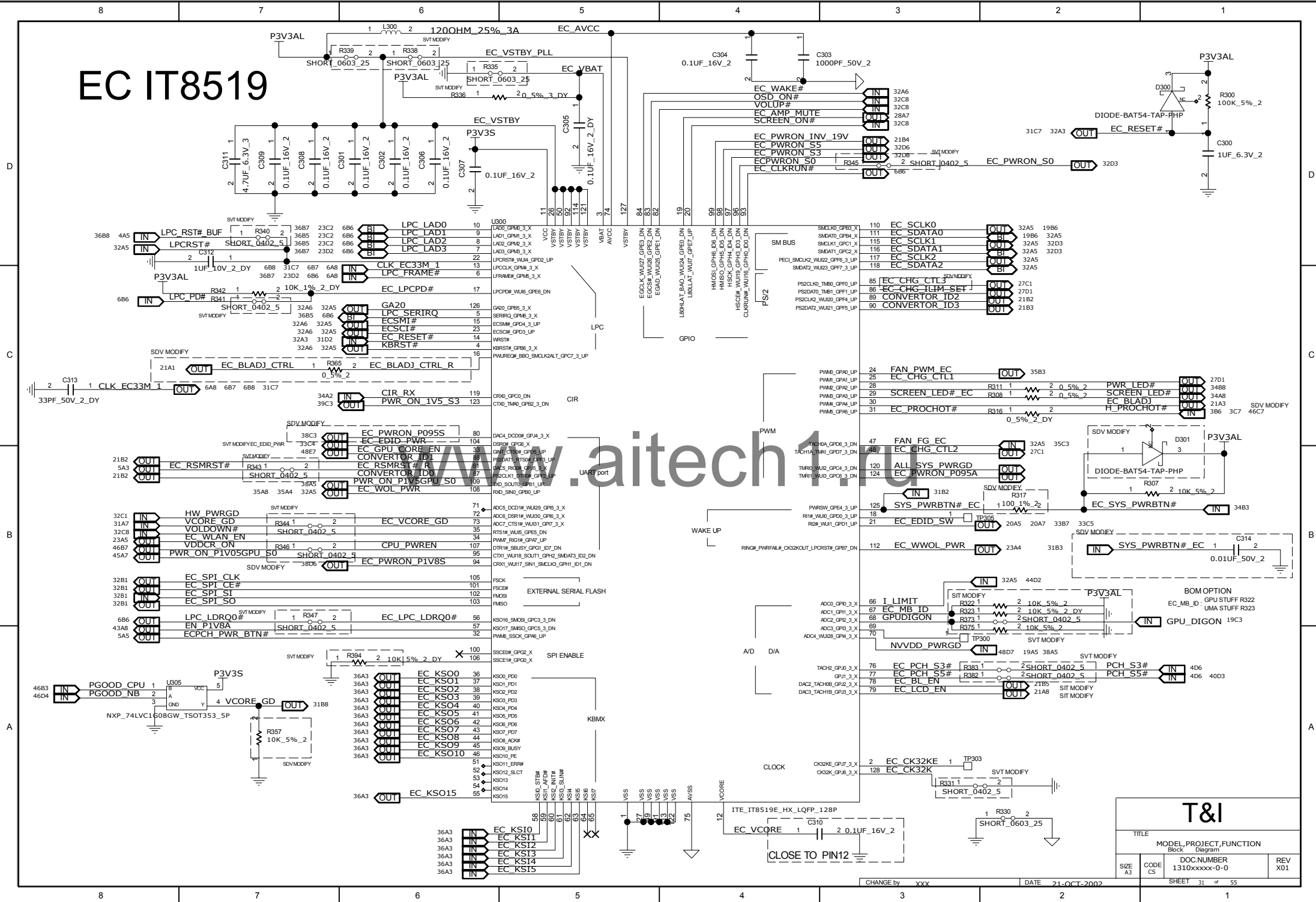
TITLE MODEL PROJECT FUNCTION Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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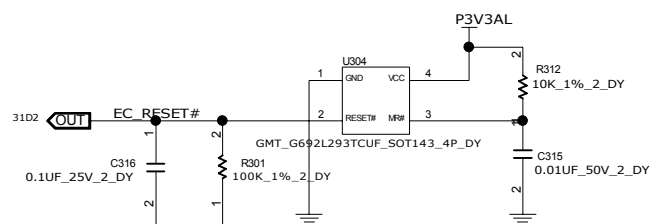
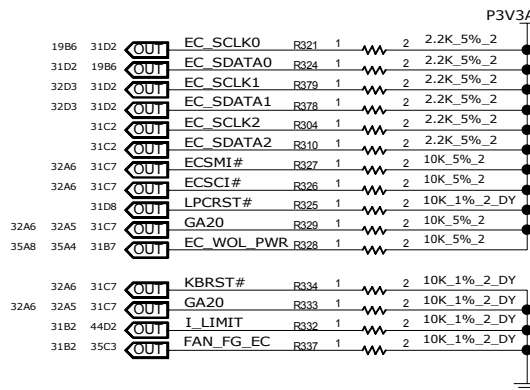
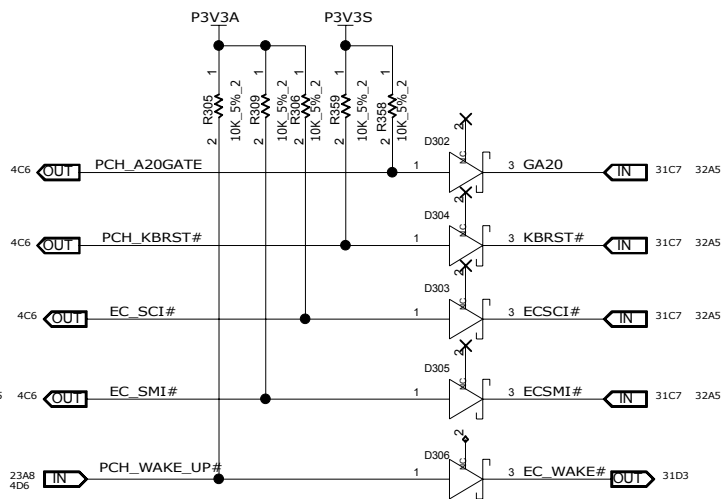
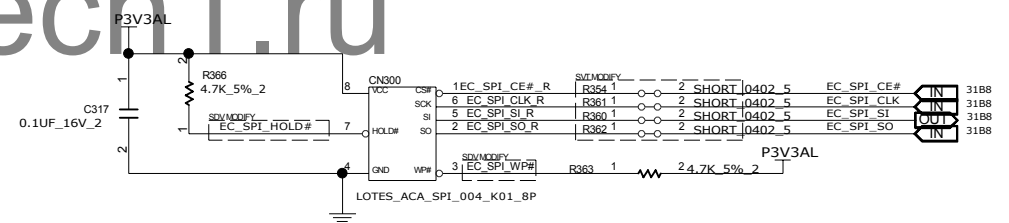
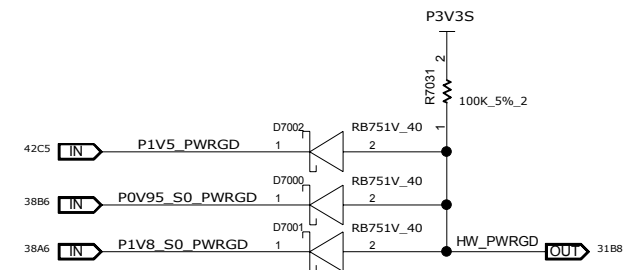
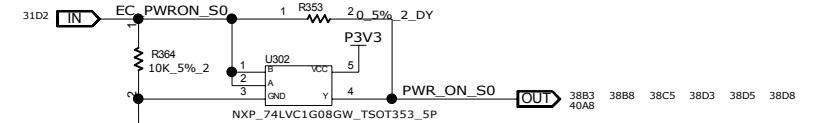
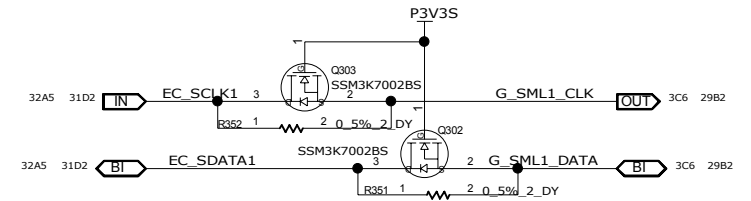
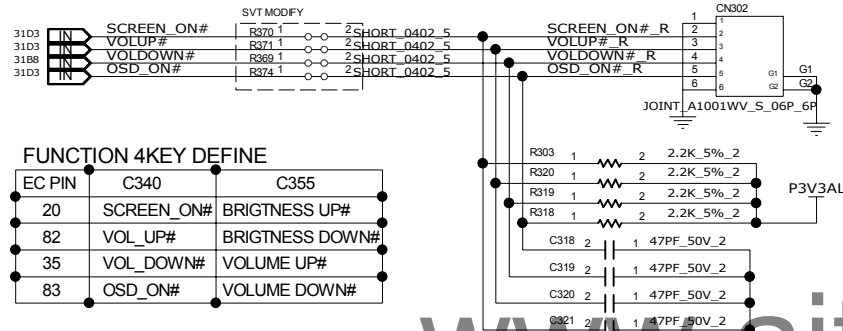
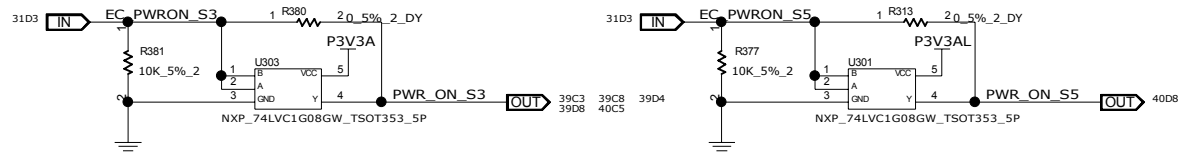
CHANGE by xxx DATE 21-OCT-2002

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# EC IT8519



# EC IT8519 / FUNCTION KEY CONN



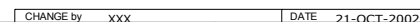
T&I				
TITLE				
MODEL PROJECT FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	

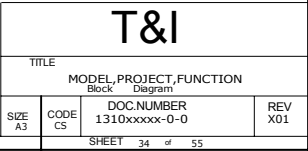
CHANGE by xxx DATE 21-OCT-2002

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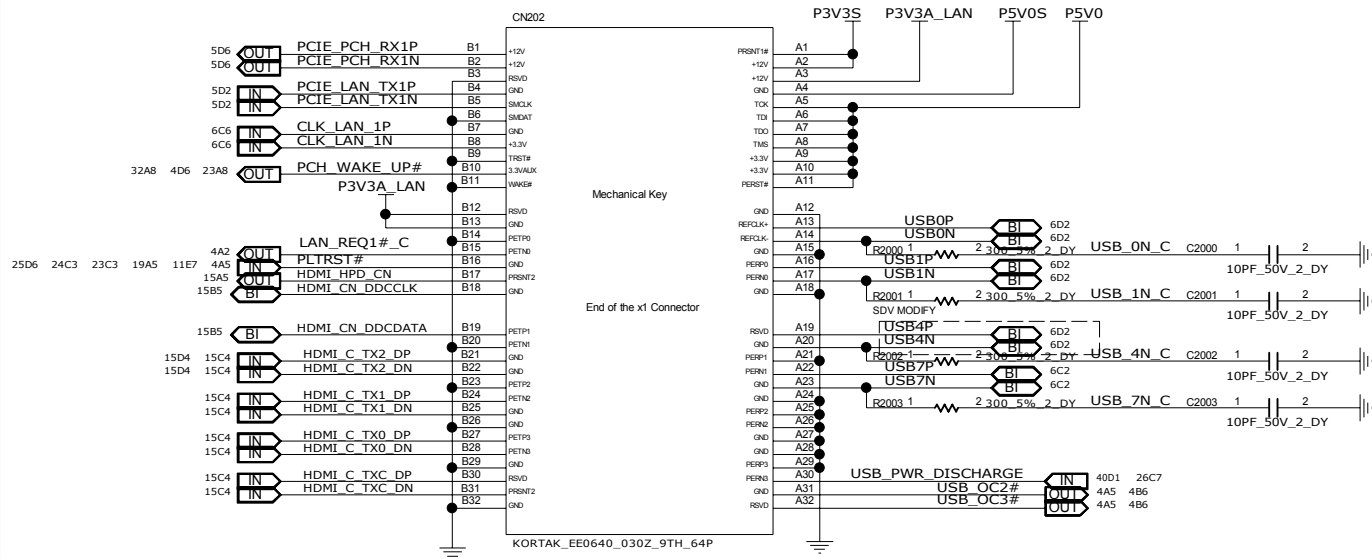
## A



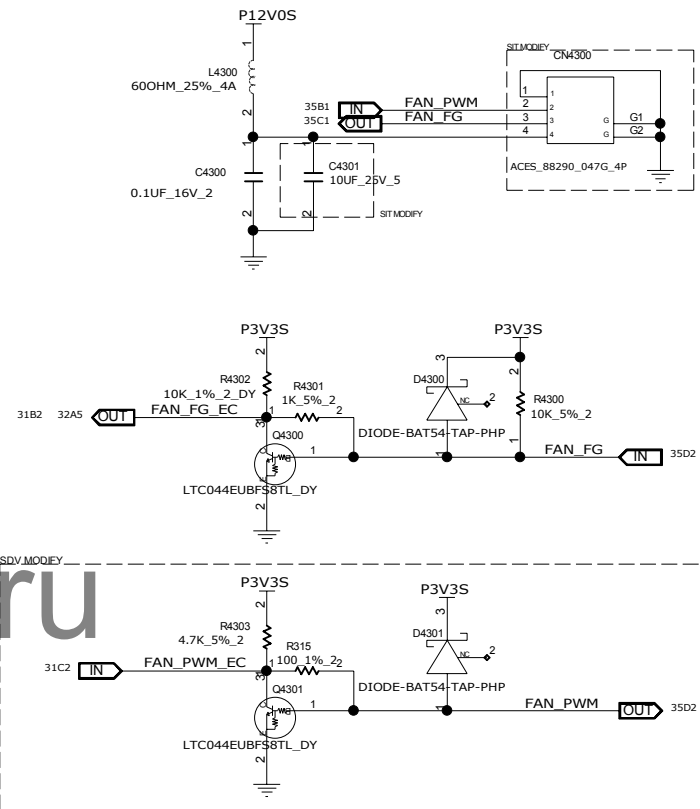


CHANGE by	xxx	DATE	21-OCT-2002
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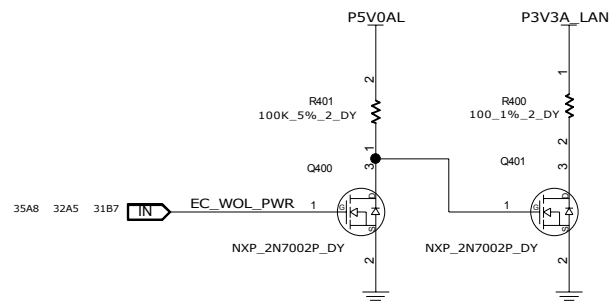
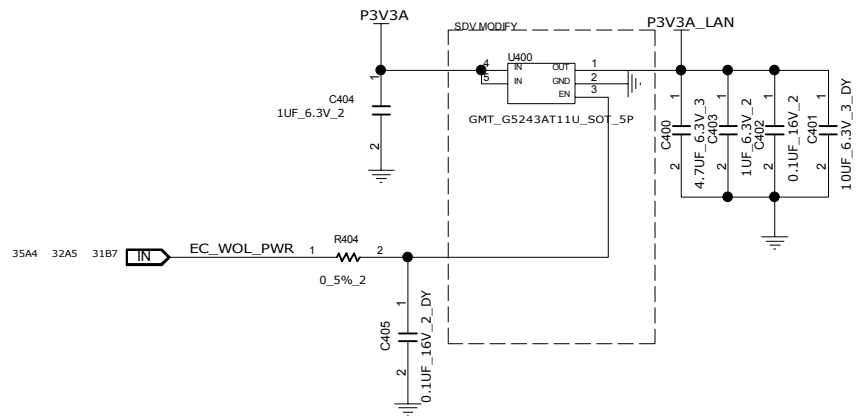
# REAR IO



# FAN CONTROL



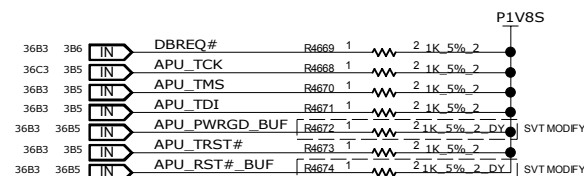
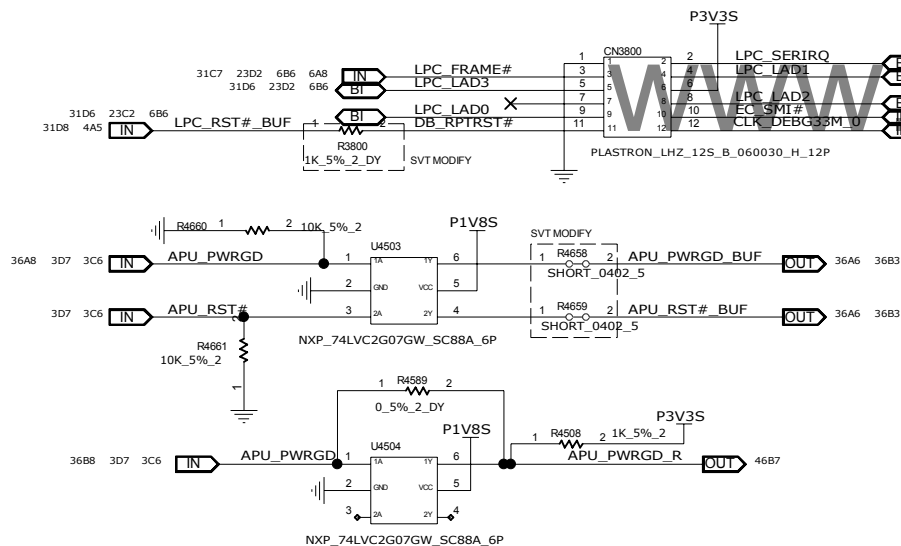
# LAN\_VDD33 DISCHARGE



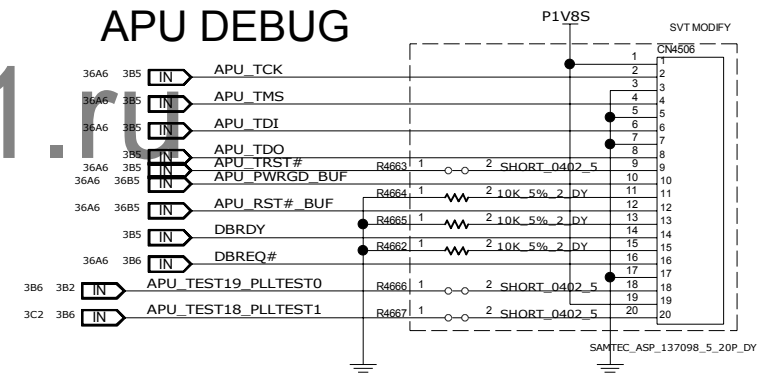
<h1>T&amp;I</h1>			
TITLE			
MODEL, PROJECT, FUNCTION Block          Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0	REV X01
SHEET    35    of    55			

D

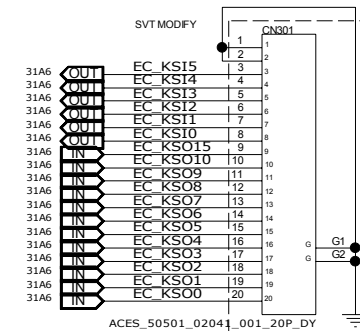
## LPC DEBUG PORT



# APU DEBUG



## EC DEBUG PORT



<h1 style="margin: 0;">T&amp;I</h1>			
TITLE MODEL, PROJECT, FUNCTION Block      Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET      26   of   66			

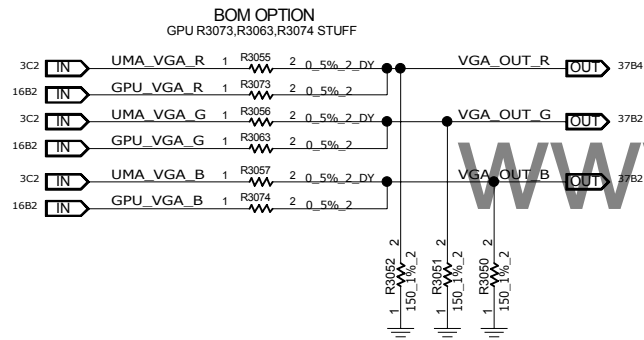
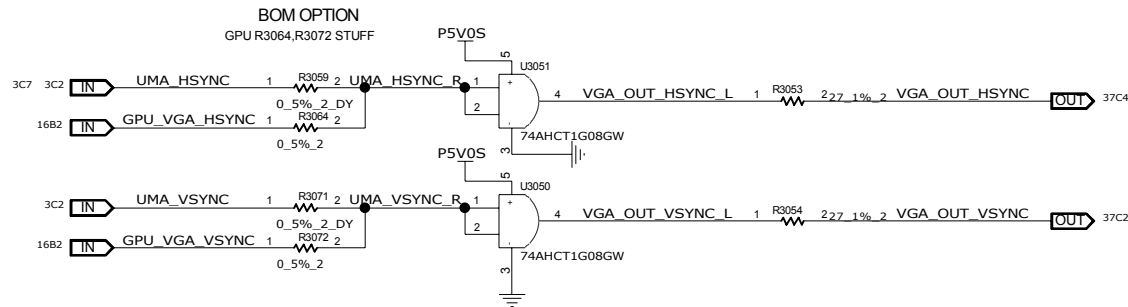
CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 36 of 55

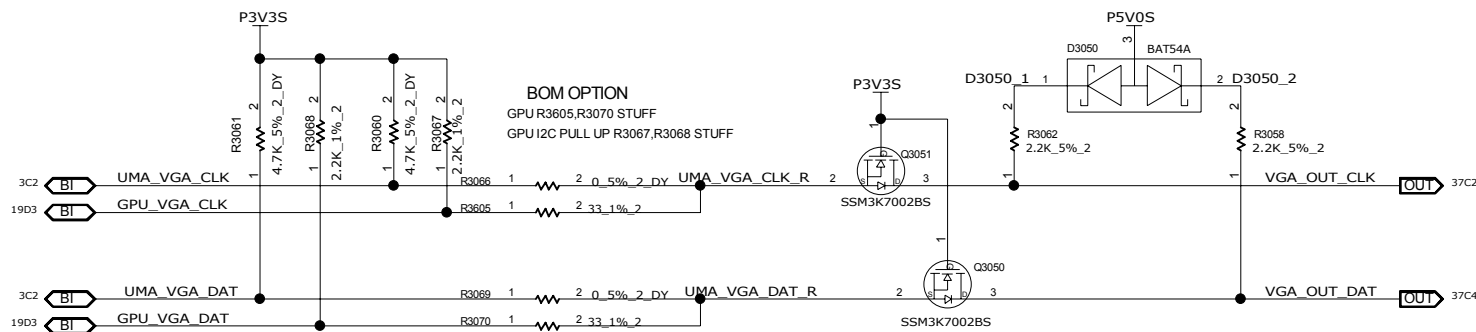
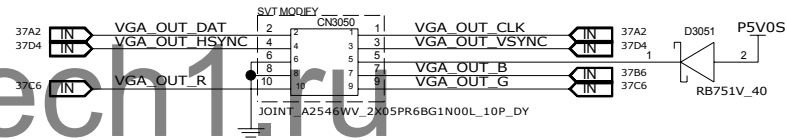
B

A

# DEBUG FUNCTION CONNECTOR



## VGA DEBUG PORT



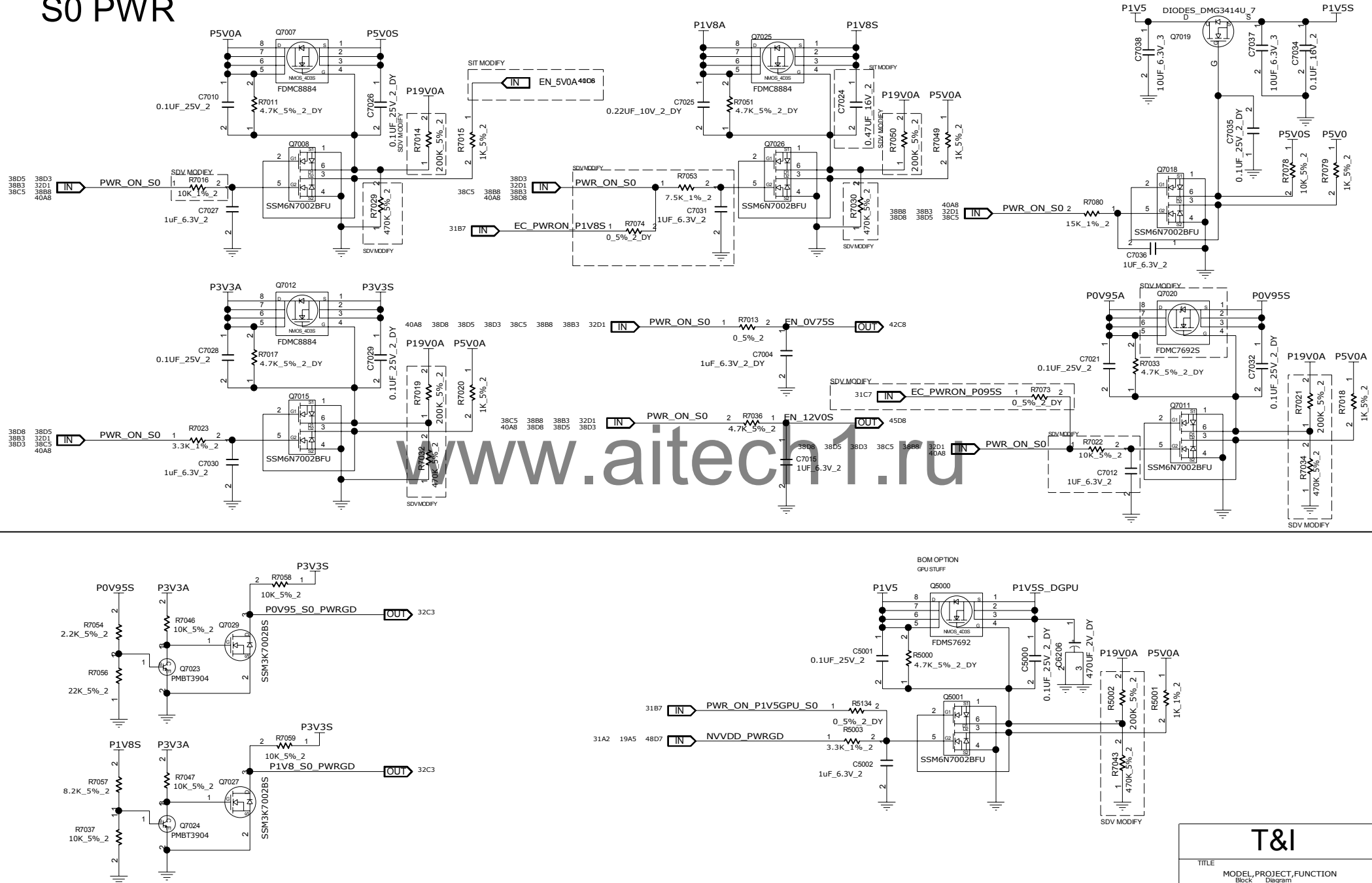
**INVENTEC**

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

CHANGE by xxx DATE 21-OCT-2002

SHEET 37 of 55

# S0 PWR

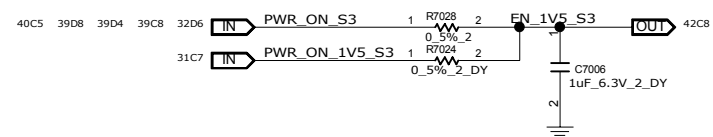
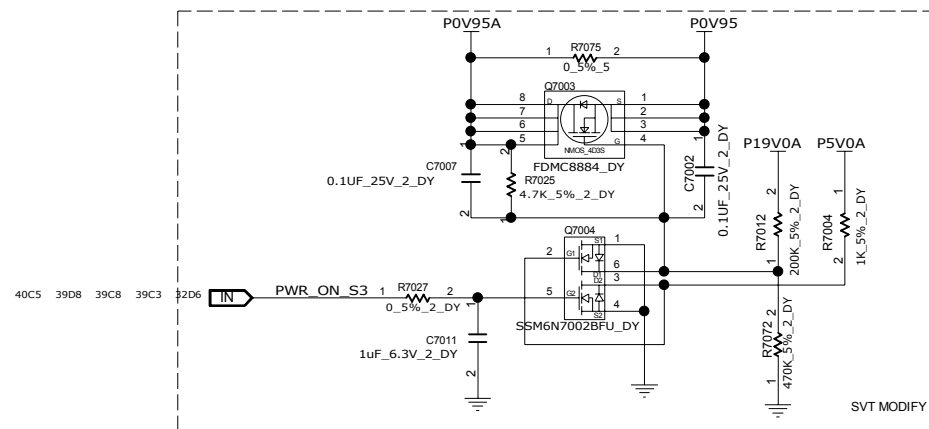


T&I

TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOCNUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by xxx DATE 21-OCT-2002

SHEET 38 of 55

[illegible]

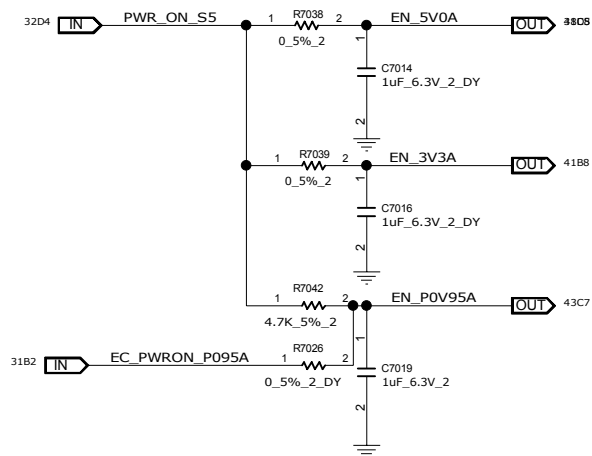
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<h1 style="margin: 0;">T&amp;I</h1>			
TITLE			
MODEL, PROJECT, FUNCTION Block                  Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET    20    of    55			

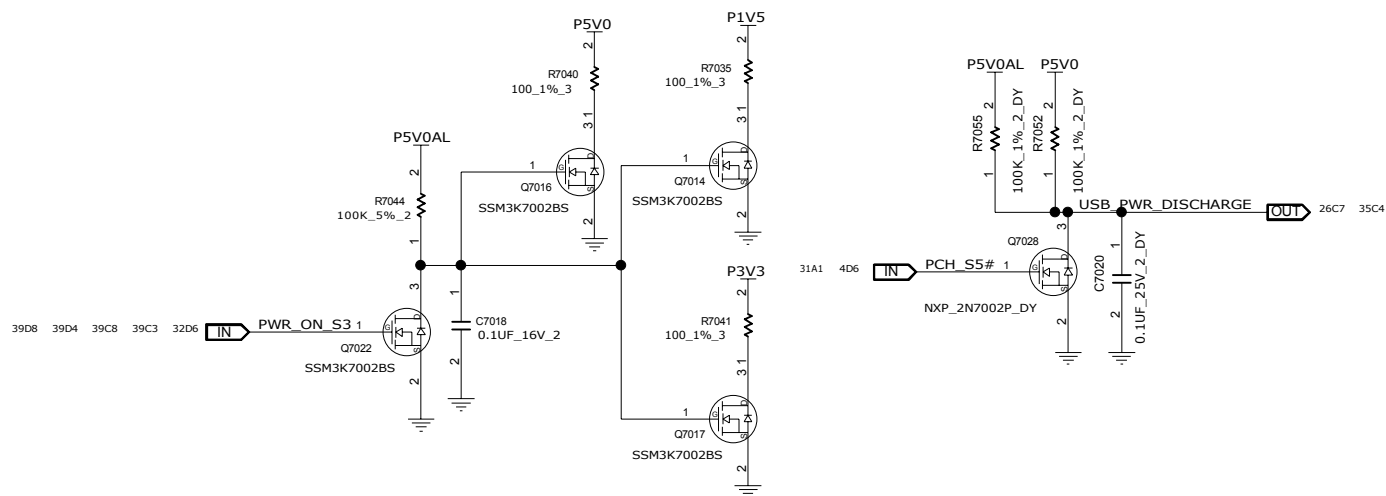
CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 39 of 55

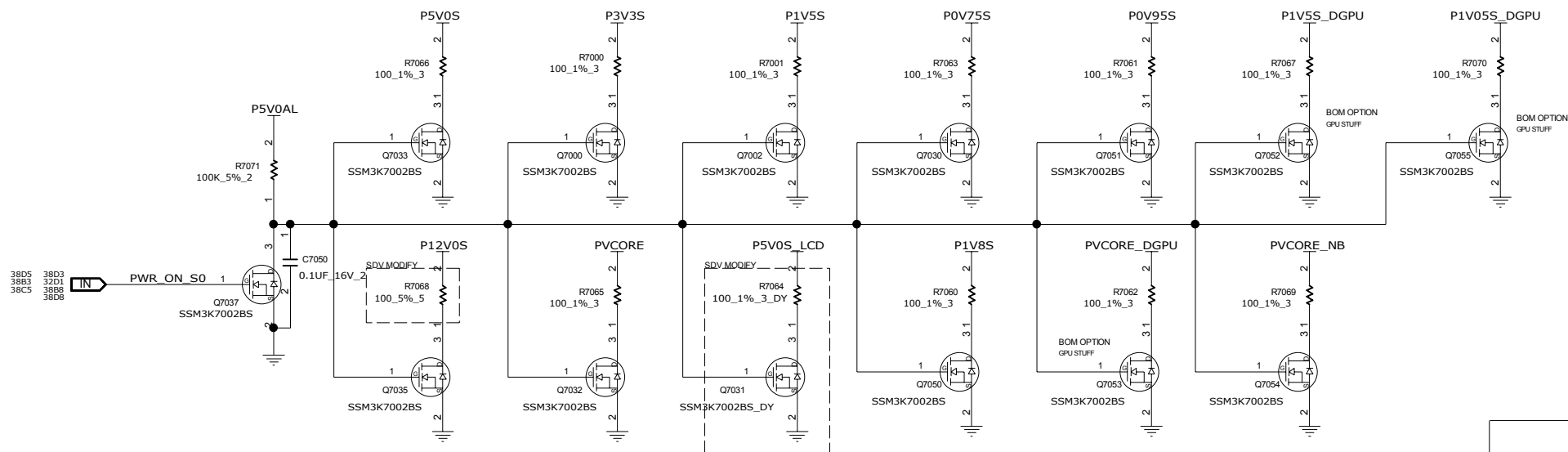
# S5 PWR



## DISCHARGE CIRCUIT



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T&amp;I

TITLE	MODEL,PROJECT,FUNCTION
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SIZE A3	CODE CC	DOC. NUMBER 1310xxxxx-0-0	REV X01
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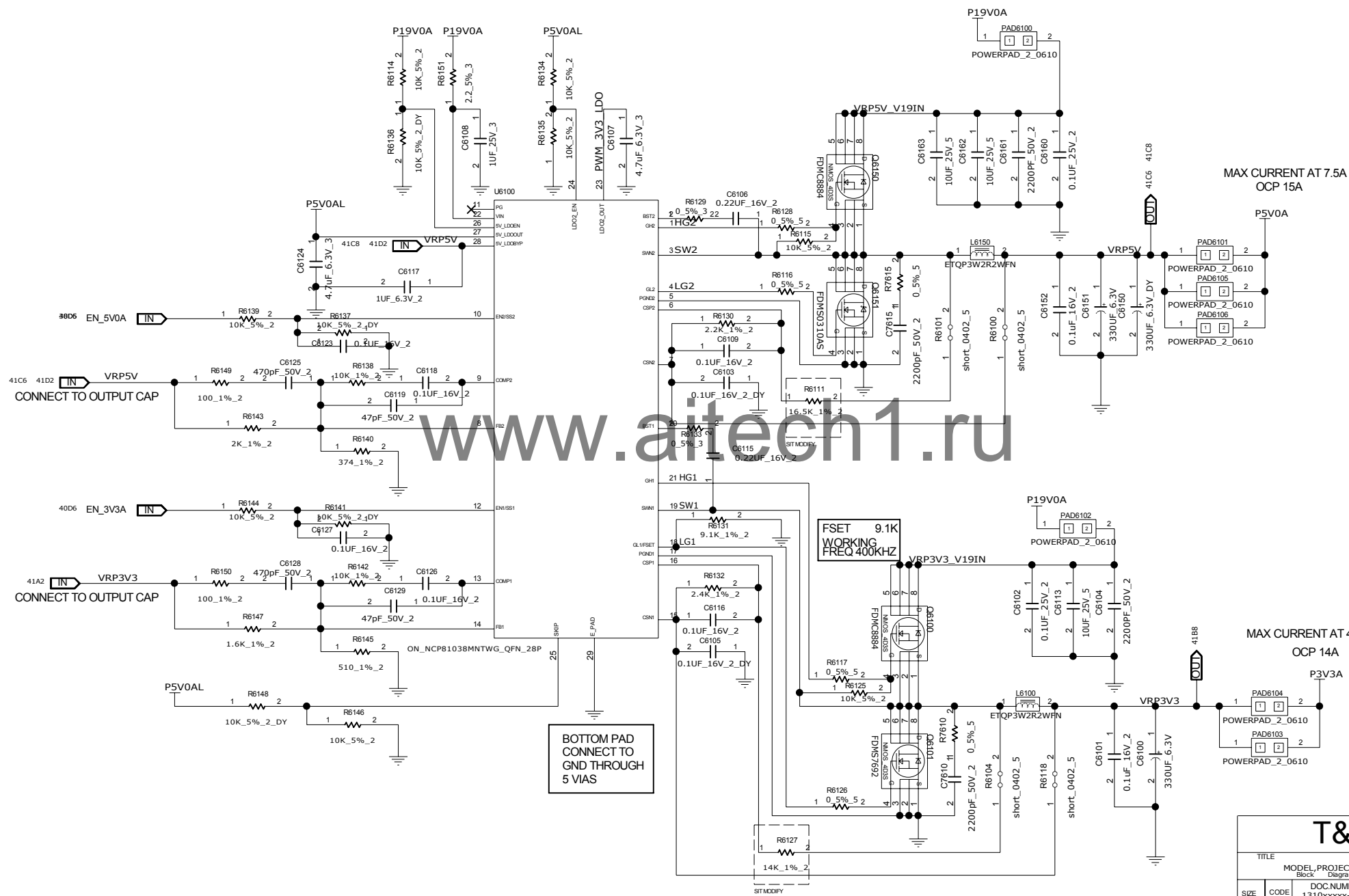
SHEET 40 of 51

CHANGE by	yyy	DATE	31-OCT-2003
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SHEET 40 of 51



## +3V\_S5 & +5V\_S5

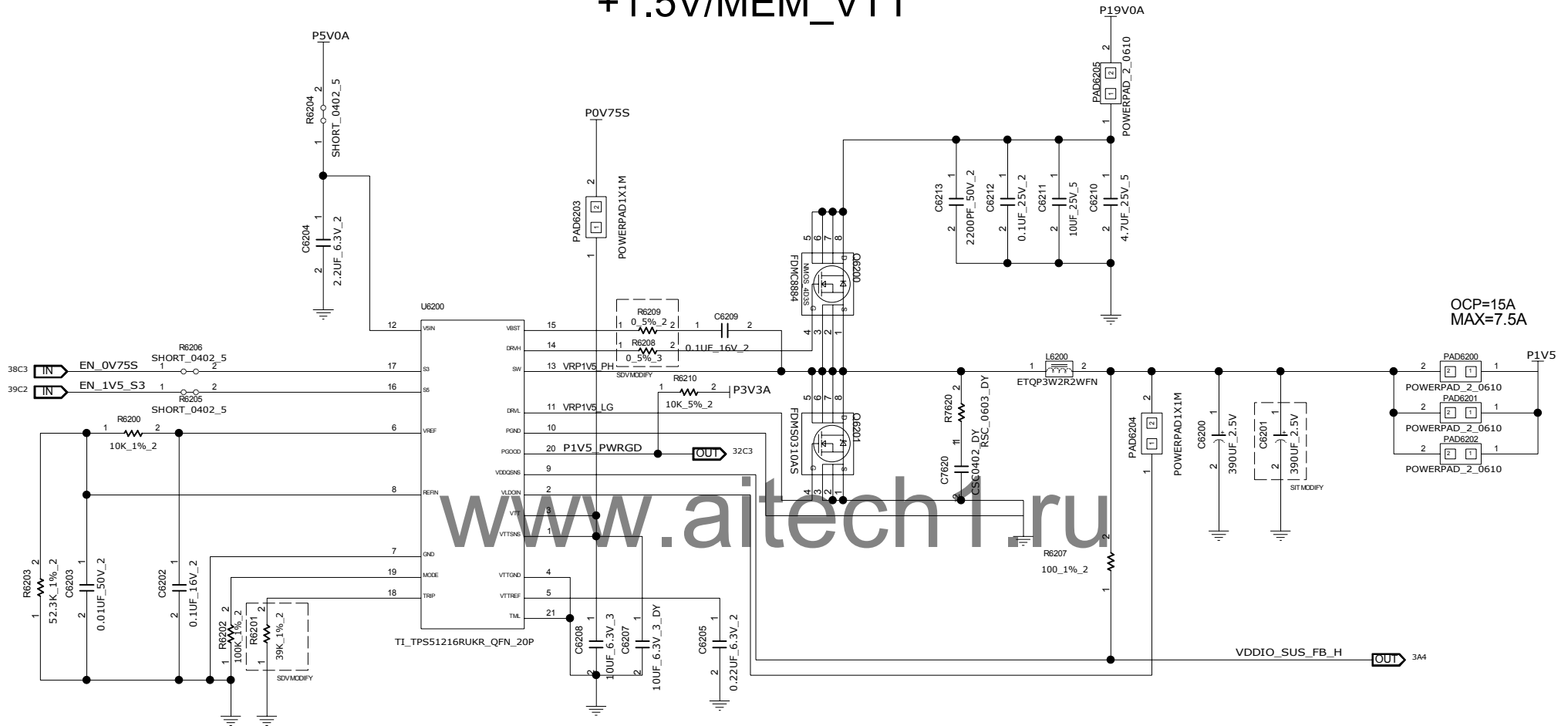


T&amp;I

TITLE			
MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 41 of 55			

CHANGE by	XXX	DATE	21-OCT-2002
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# +1.5V/MEM\_VTT



OCP=15A  
MAX=7.5A

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

T&I

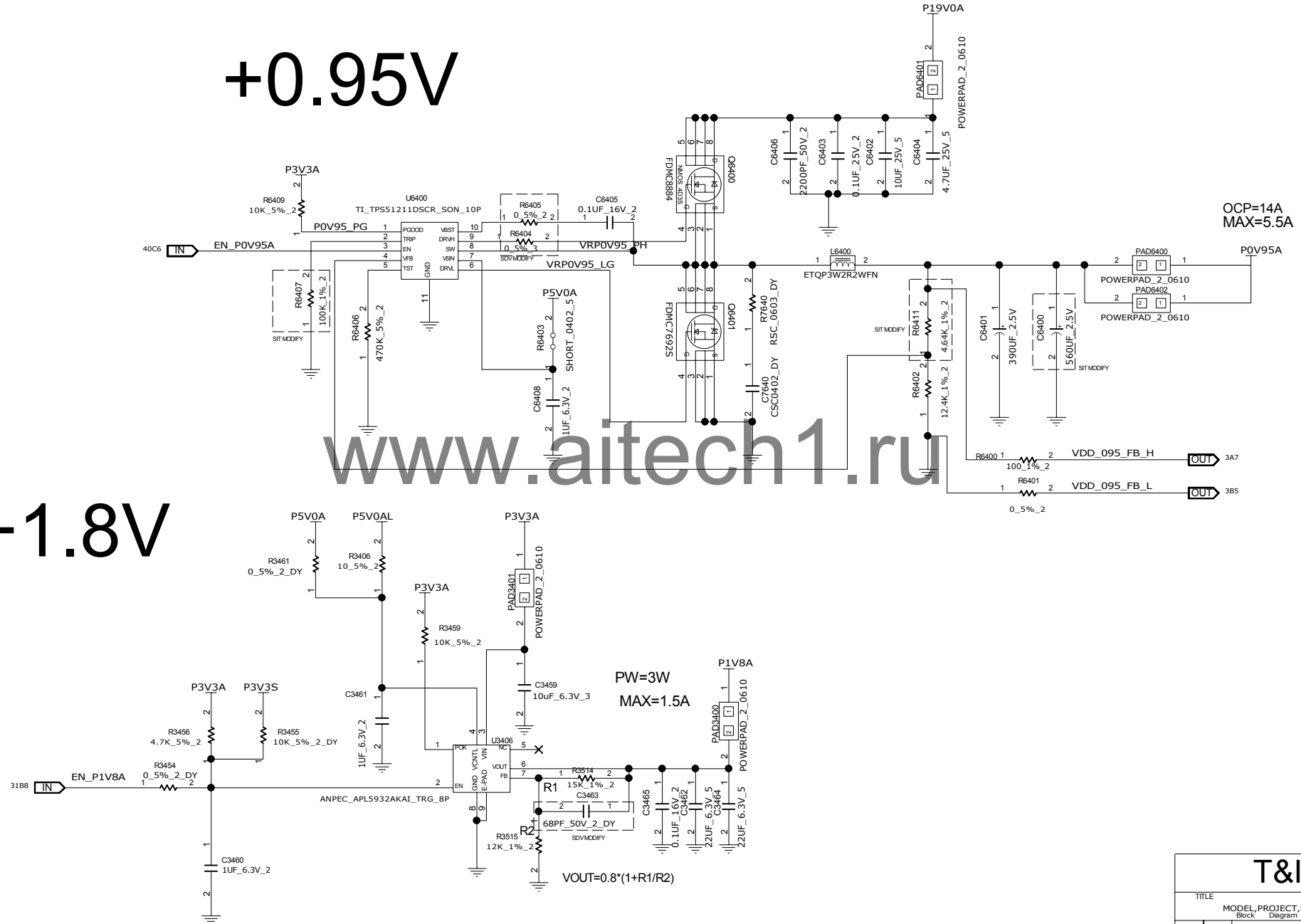
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

CHANGE by: xxx DATE: 21-OCT-2002

SHEET 42 of 55

+0.95V

+1.8V

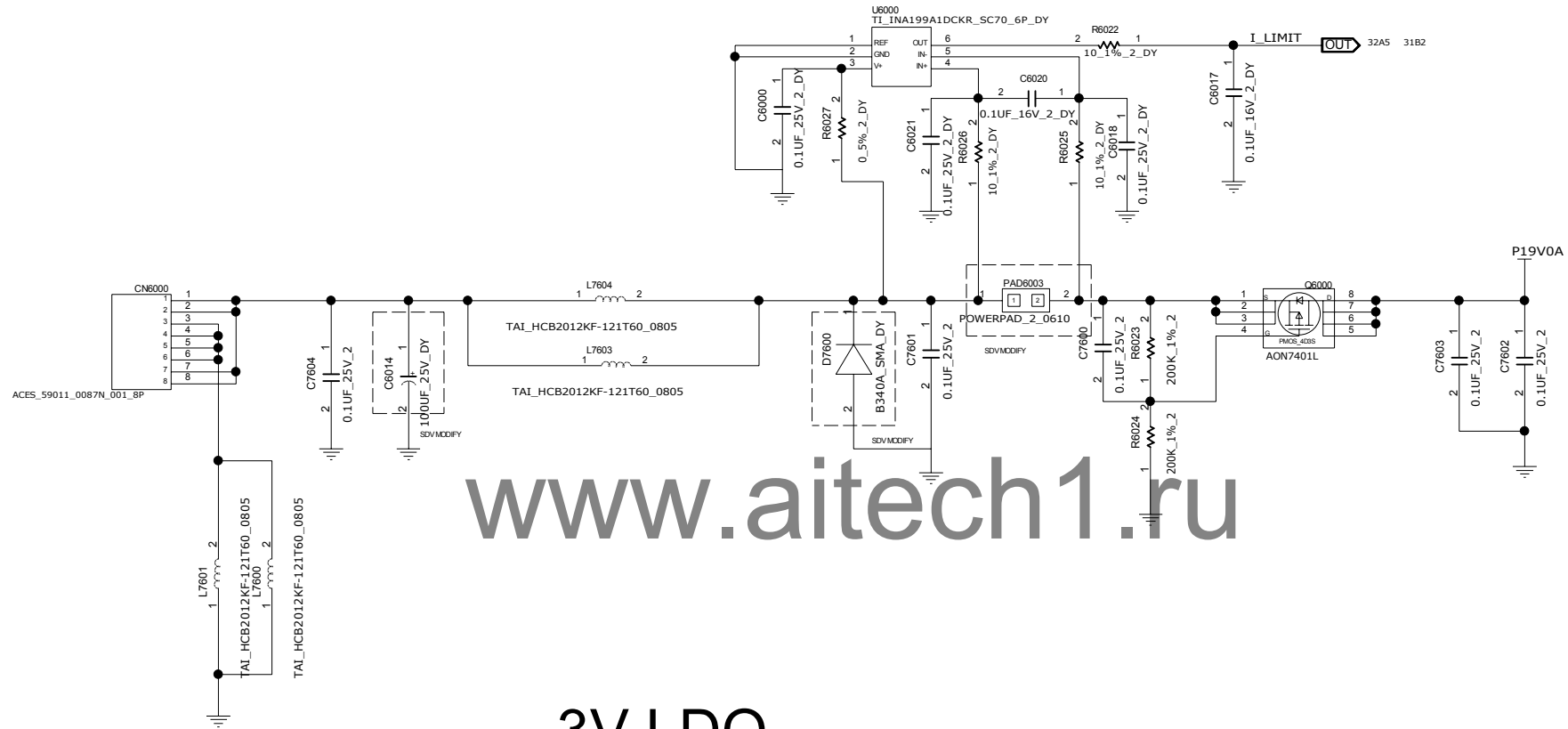


T&I			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 43 of 55

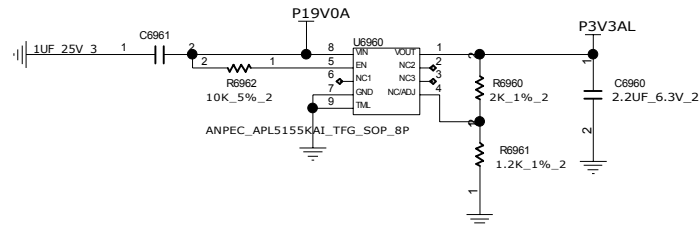
# DC-IN



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## 3V LDO

PW=2W  
MAX=0.1A



T&I

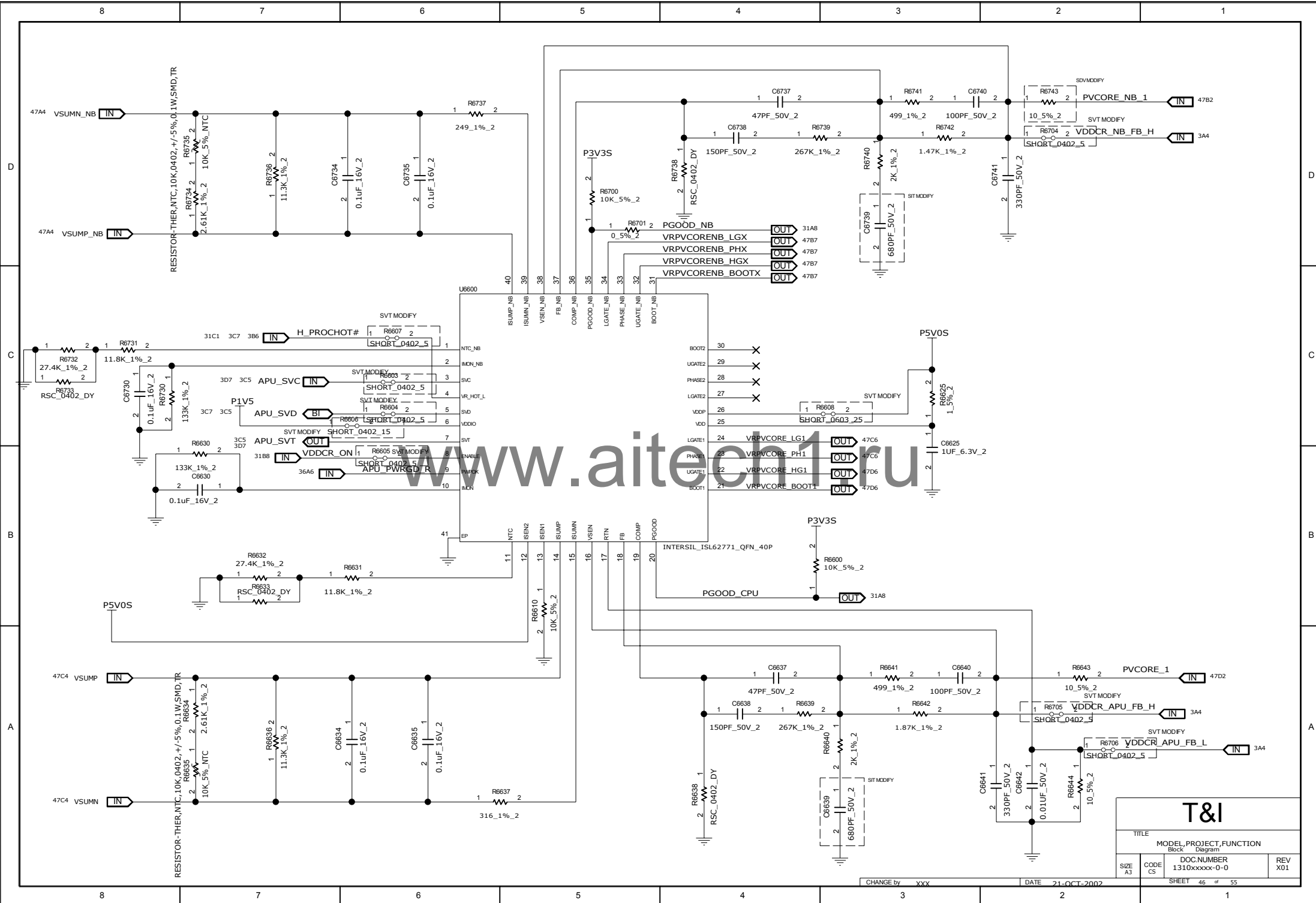
TITLE  
MODEL, PROJECT, FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by xxx DATE 21-OCT-2002

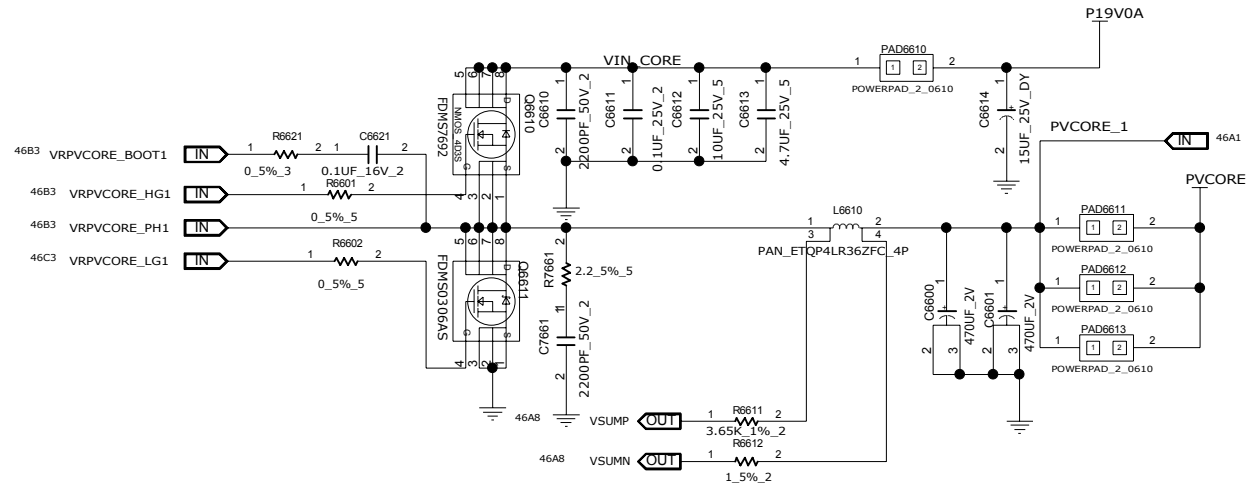
SHEET 44 of 55



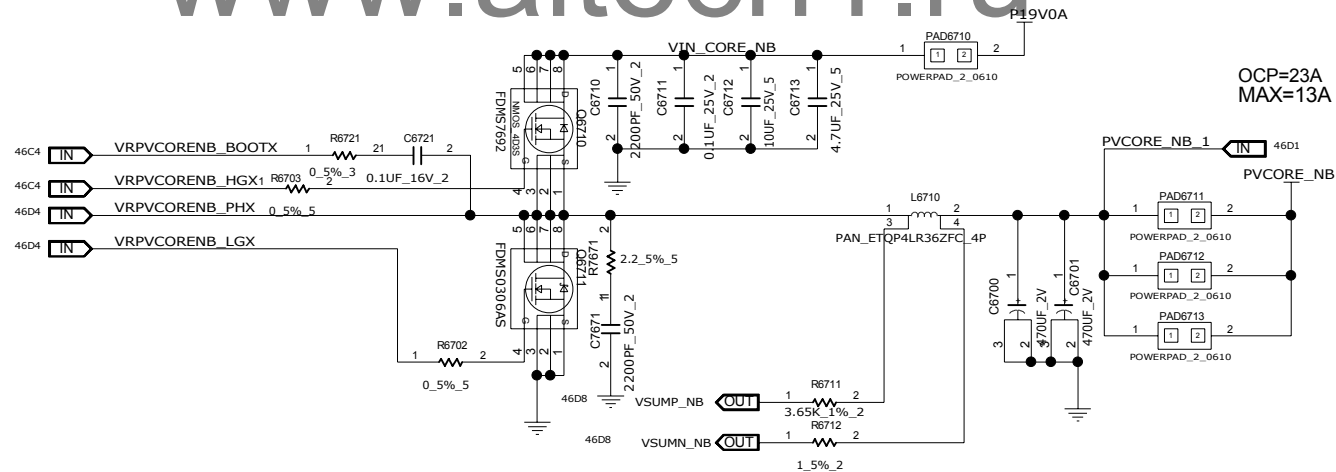


# 62771 OUTPUT

OCP=28.8A  
MAX=15A



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OCP=23A  
MAX=13A

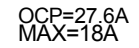
T&I

TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by xxx DATE 21-OCT-2002

SHEET 47 of 55

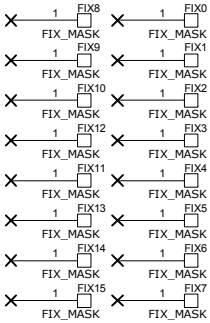
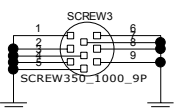
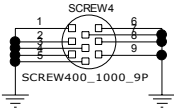
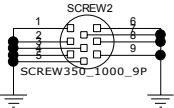
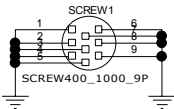
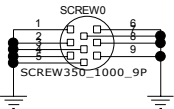
BOM OPTIC  
GPU STUFF



TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 48 of 55			



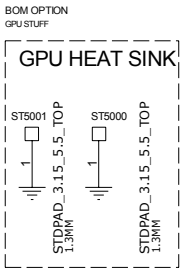
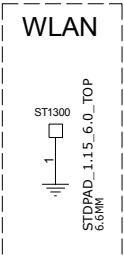
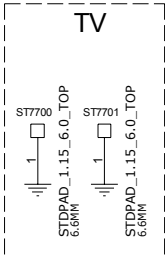
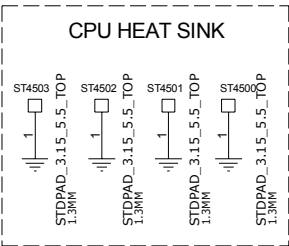
SCREW



需備料  
COIN BATTERY 6027B0009101  
EC ROM 6019B0719601(8M BIT)  
SYSTEM ROM HIGH SPEED 6019B1039501(32M BIT)  
JUMPER X2 6012B0134303  
PCB 185X190 6050A259601

REMARK  
IF U2500 NEED POP COMONENT, USE 6019B1035901(TPS2546RTER) FOR METERIAL  
DDR SOCKET, CN4101:6026B0180001(H8), CN4100:6026B0121002(H4)  
LPC DEBUG PORT (CN3800) CHANGE TO 6012B0517501  
VGA DEBUG PORT (CN3050) CHANGE TO 6012B0517502

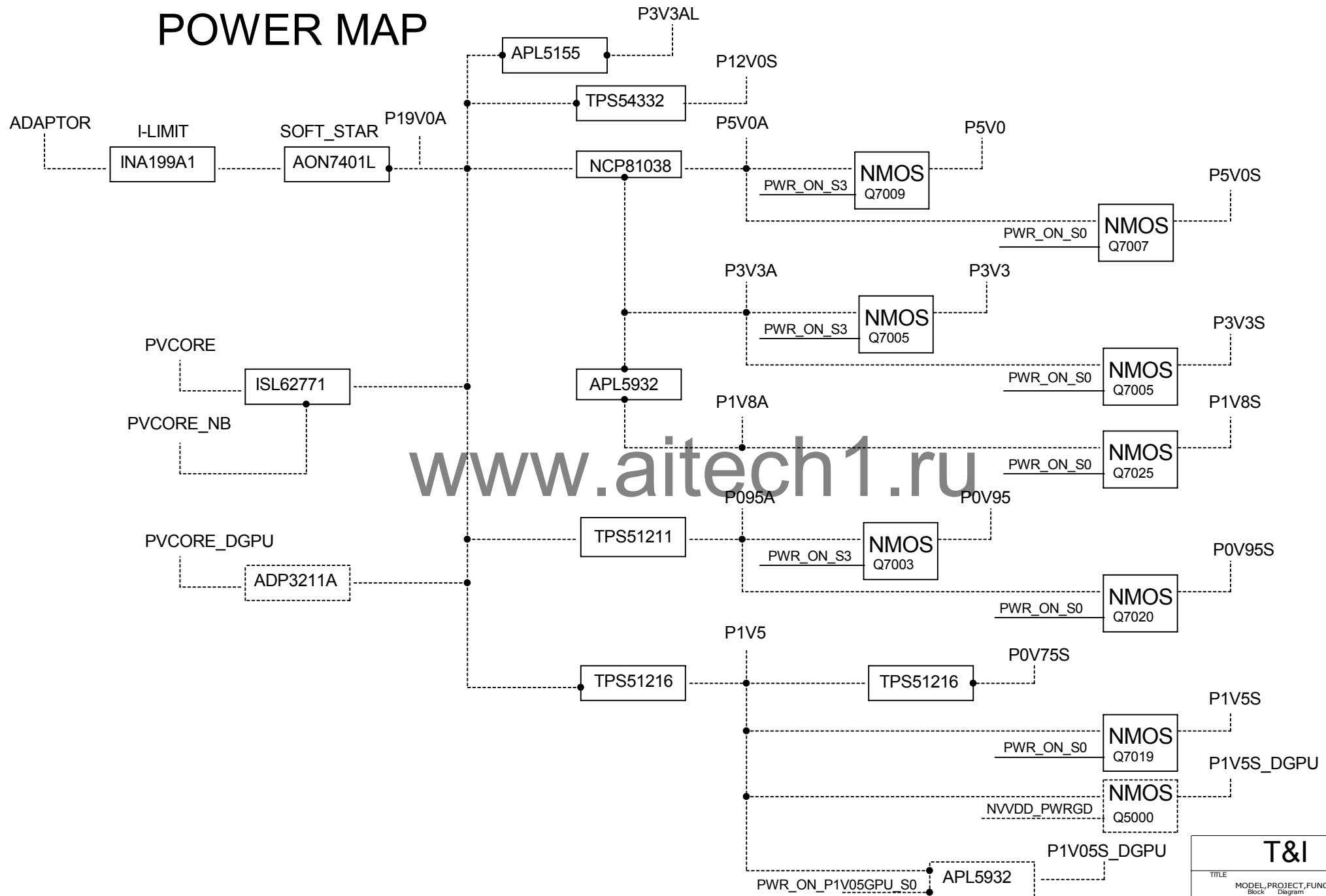
www.aitech1.ru  
STAND OFF



INVENTEC

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

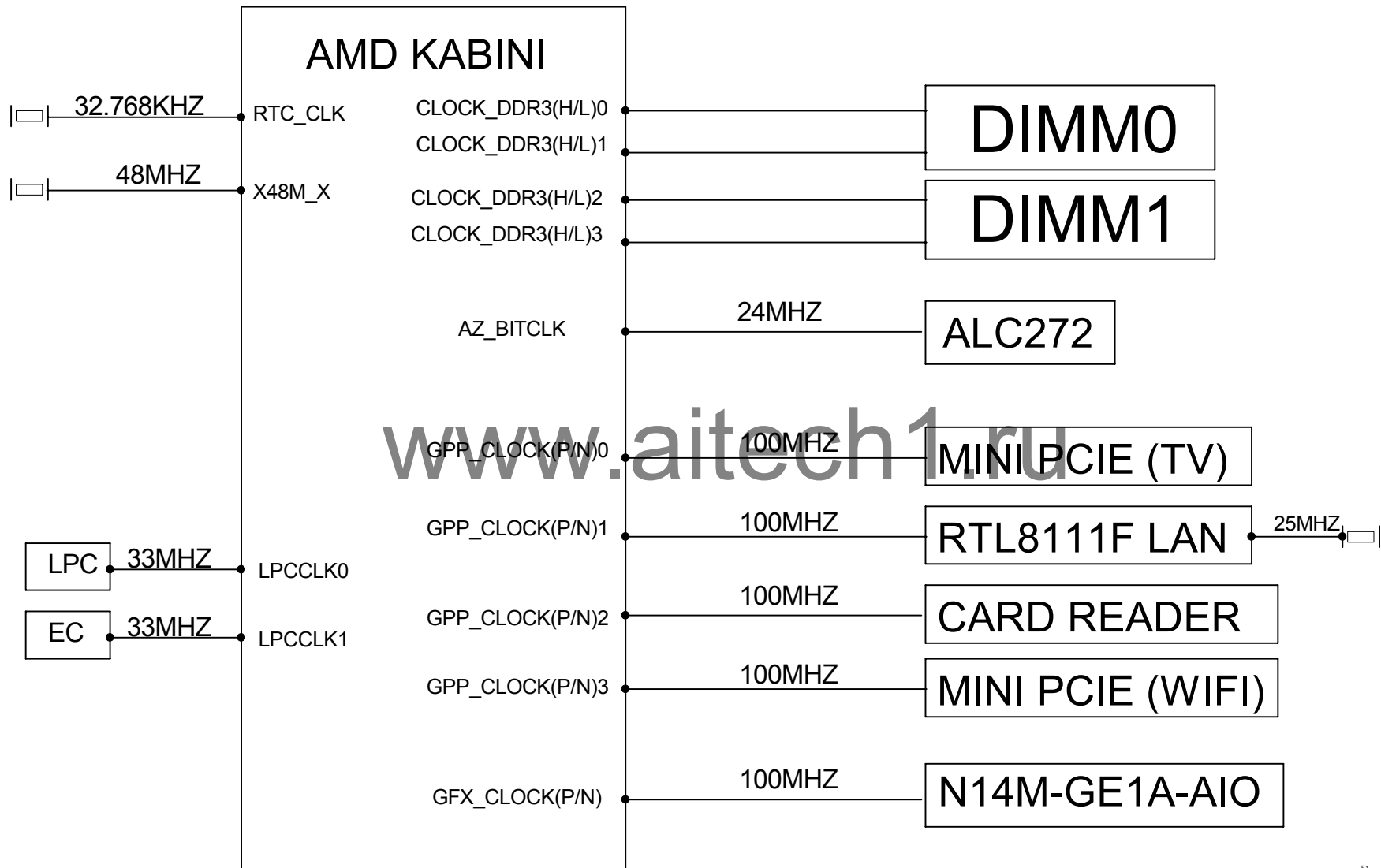
# POWER MAP



www.aitech1.ru

T&I			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 50 of 55			

# CLOCK MAP



51

T&I

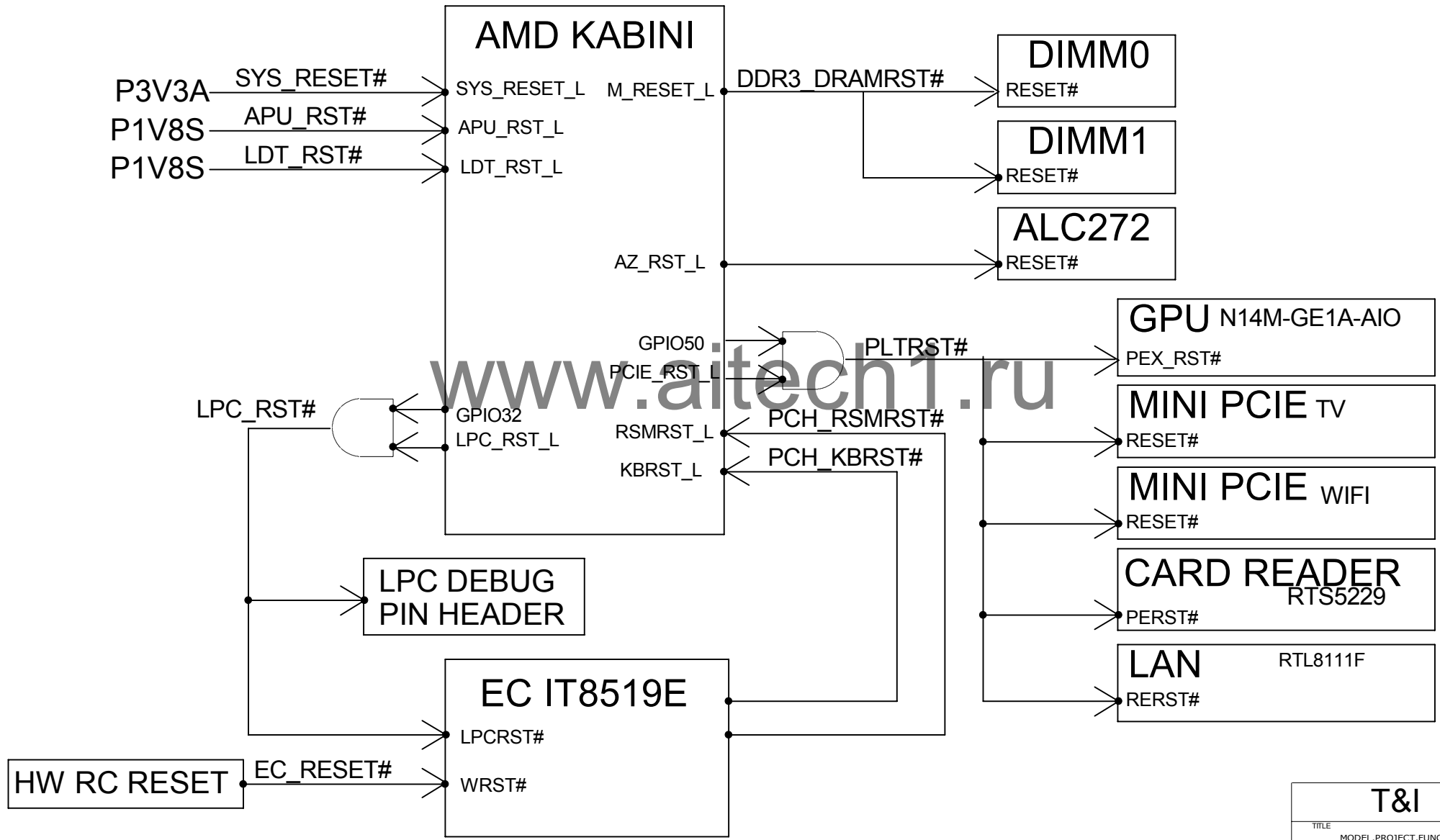
TITLE  
MODEL, PROJECT, FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by: xxx DATE: 21-OCT-2002

SHEET 1 of 55

# RESET MAP



T&I			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

# APU GPIO TABLE

GPIO	FUNCTION	TYPE	POEWR WELL
GPIO 32	SB_ARST#_GATE	IO	MAIN
GPIO 33	NC	IO	MAIN
SMBus Clk 0 / GPIO 43	DDR_CLK	IO	MAIN
GPO 45	NC	O	MAIN
SMBus Data 0 / GPIO 47	DDR_DAT	IO	MAIN
Serial IRQ for DDMA / GPIO48	LPC_SERIRQ	IO	MAIN
GPIO49	NC	IO	MAIN
GPIO50	PCIE_RST#_GATE	IO	MAIN
GPIO51	NC	IO	MAIN
GPIO52	NC	IO	MAIN
GPIO55	NC	IO	MAIN
GPIO56	NC	IO	MAIN
GPIO57	NC	IO	MAIN
GPIO58	NC	IO	MAIN
GPIO59	NC	IO	MAIN
GPIO60	TV_REQ0#	IO	MAIN
GPIO61	LAN_REQ1#	IO	MAIN
GPIO62	CR_REQ2#	IO	MAIN
GPIO63	WLAN_REQ3#	IO	MAIN
GPIO64	NC	IO	MAIN
GPIO65	NC	IO	MAIN
GPIO66	PCH_BEEP	IO	MAIN
GPIO67	SATA_LED#	IO	MAIN
GPIO68	TP4513	IO	MAIN

GPIO69	TP4519	IO	MAIN
GPIO70	NC	IO	MAIN
GPIO71	NC	IO	MAIN
GPIO73	CLR_PASSWORD#	IO	MAIN
GPIO74	NC	IO	MAIN
GPIO75	NC	IO	MAIN
GPIO76	NC	IO	MAIN
GPIO77	NC	IO	MAIN
GPIO78	NC	IO	MAIN
GPIO79	NC	IO	MAIN
GPIO80	NC	IO	MAIN
GPIO161	PCH_SPI_WP#	IO	SUS
GPIO162	PCH_SPI_CLK	IO	SUS
GPIO163	PCH_SPI_DATAOUT	IO	SUS
GPIO164	PCH_SPI_DATAIN	IO	SUS
GPIO165	PCH_SPI_CS0#	IO	SUS
GPIO166	TP4515	IO	SUS
GPIO167	PCH_HDA_SDIN0	IO	SUS
GPIO168	PCH_HDA_SDIN1	IO	SUS
GPIO169	PCH_HDA_SDIN2	IO	SUS
GPIO170	PCH_HDA_SDIN3	IO	SUS
GPIO174	TP4520	IO	SUS
Infrared LED / Low Low Battery / GPIO184	CLR_CMOS	IO	SUS
SMBus Clk 1 / GPIO 227	PCH_SMBCLK	IO	SUS
SMBus Data 1 / GPIO228	PCH_SMBDATA	IO	SUS

T&I

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 53 of 55			

CHANGE by: xxx DATE: 21-OCT-2002

